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ADDRESSABLE TIME DIVISION MULTIPLEXER SYSTEM

(CABLE AND CONNECTOR STUDY)

MCR-67-425

FINAL REPORT

DECEMBER 1967

Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GEORGE C. MARSHALL SPACE FLIGHT CENTER
HUNTSVILLE, ALABAMA 35812

Prepared by

MARTIN MARIETTA CORPORATION
DENVER DIVISION

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DENVER DIVISION

FOREWORD AND INTRODUCTION

The Denver Division of the Martin Marietta Corporation performed early in-house studies of distributed multiplexer systems and later continued these studies under contract to NASA-MSFC. The results of these programs, which included the development of prototype equipment for NASA, have demonstrated system feasibility using single interrogation cables and single data cables to interconnect several multiplexers to a central control unit. Though studies have covered the problems of the system and the development of equipment rather thoroughly, a need has existed for further study of the role of the interconnecting cables. This final report which is a result of the study undertaken under contract NAS 8-21176 attempts to relate cables and connectors to the rest of the system in true perspective.

Our report discusses the state-of-the-art of cables and connectors. We have analyzed cables with multiple loads and various terminations with respect to the applications of transient (pulse) voltages. The analyses have been supported by general laboratory tests and we have further demonstrated the properties of the cables in a typical distributed multiplexer system. As a result, information is presented for the selection of cables and connectors to fit a particular application. Much of the report is devoted to an overall system reliability study which shows how the system and interconnecting cables affect reliability figures. Various arrangements are studied in hopes that the reader may compare the effects of adding redundancy and other system complexities to potential improvements in reliability. It is believed that final choice of a system must be predicated upon mission goals.

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LIST OF FIGURES

I. CABLE AND CONNECTOR STATE-OF-THE-ART

If one is to make appropriate recommendations for the selection and proper application of cables and connectors to the Addressable Time Division Data Systems a good knowledge of the state-of-the-art must be established. A search for written literature, establishment of vendor contacts, a review of manufacturing techniques and a look at R and D all seem advisable. We have attempted to pursue these avenues.

A. LITERATURE SURVEY

A bibliography was obtained from a NASA literature search of the Defense Documentation Center, and library searches by several Martin Marietta personnel. Areas searched concerning cables and connectors were; rf, coaxial, shielded twisted pair, reliability, development, testing, and applications. Perhaps cables and connectors are considered too glamourless or are taken very much matter-of-fact but only a few reports seem worthwhile. Many of the better sounding articles related to past governmental contracts are classified as "limited access" and are unavailable which further reduces the quantity of good literature.

A summary of the literature search indicates that little cable or connector research and development occurs except upon demand. The state-of-the-art consists generally of the obvious coaxial and twisted cables and connectors covered by MIL-specifications plus a few special digital cables for which no special connectors

have been developed. There is much work in printed cables, but most of this consists of the development of multi-conductor internal package harnesses, where shielding may or may not be employed, and the development of external custom multi-conductor cable assemblies (long and short) with no shielding. It has been stipulated in the past, by proponents of flat cable, that few harnesses require shielding. But where shielding is required there is no standardization. There is little indication of a present change in philosophy on shielding standardization, and it is the author's opinion that physical shortcomings of long shielded flat cables will delay standard specifications for several years. Electrical characteristics are at least equal to and probably superior to those of round cables.

There are numerous references to cable and connector testing, but most of these are qualification test reports where an item has been qualified to standard MIL-specs, rather than reports on applications that might be appropriate to this program.

A few documents are written on the development of cables and connectors, but most are classified "limited access". Although a few of these articles may be appropriate to this study, the majority appear to report on unrelated applications such as submarines, arctic, etc. Some of the unavailable material such as reports on the development of lightweight coaxial cable assemblies, and cables with plated on shields appears appropriate.

No bibliography concerning cable or connector reliability per se was discovered. Some information is contained in general reports and studies that have been written comparing solder, crimp, and welded connections, but our survey cannot reference one good document on the subject other than the reliability analyses which we are reporting herein.

We found no articles on cables and connectors and their specific application to pulse circuits, but there were several articles (other than books on transmission theory) regarding Electromagnetic Interference (EMI) considerations such as grounding practices, shielding techniques, cable terminations, and cable losses. Much of this data is useful in pulse applications. One article (4) regarding grounding and shielding was reported upon in Monthly Progress Report MCR-67-266 (Issue I) (1). Another paper (5) concerning the same subject compares the shielding effectiveness of shielded twisted pair and coaxial cable with much the same results. It is stated that the shielded twisted pair can provide approximately 20 db attenuation of frequencies below 5kHz with the twisting providing most of the attenuation to the magnetic fields that exist. A typical copper braid shield as used on a coaxial cable will provide typically 40 db of attenuation at 1 mHz and will drop to less than 10 db attenuation at 20 kHz. Multipoint grounding is most effective at higher frequencies unless ground currents producing strong magnetic fields are exceptionally

high. Single point grounds are considered good for short cables, but for long cables a single point ground loses its effectiveness because of obvious attenuation of the ground path. Long cables should be grounded about every 0.15 λ where λ is the shortest wave length to be carried. Good practical grounding may be a matter of experimentation and compromises. Other literature reviewed was redundant or inconclusive.

B. MANUFACTURER'S SURVEY

The cable and connector manufacturer's survey was initiated by selecting a substantial (approximately 20) list of vendors from the various buyer guides. Companies selected were listed as manufacturing any one or all of the following items:

coaxial cable

twisted conductor cables

rf cable

flat cable

associated connectors

While some catelog data was available and reviewed for several companies, only eight of the companies had local representation. Direct contact was restricted to these eight vendors. While most of the representatives were quite cooperative they were generally uninformed other than to supply catalog data. This problem necessitated telephone calls direct to factories. Since large purchase orders are not a potential part of this study

inquiries for technical information generally received a cool reception. However, we were able to select representative companies of all products where response to inquiries was excellent. Amphenol (manufacturing coaxial cable, twisted conductor cables, and various rf cables plus a large line of connectors), Methode, and EMI (manufacturing flat cable) were chosen for a survey trip. The results of this trip was reported upon in Monthly Progress Report MCR-67-266 (Issue 2) but a summary of major points is repeated here:

> There seems to be no great effort being made in the development of specialized round cables and connectors specifically for aerospace. While only one company is directly represented in this statement, other contacts and extensive competition are indicative of an industry-wide trend. The companies are very receptive to development programs, but many MIL-items are already known to be adequate for space applications and not much work is likely in this area in the near future. Minor modifications in connectors and cables such as changing dielectric from polyethylene to teflon is a routine occurrence. The selection of coaxial cables, both standard and subminiature, and connectors for shielded application is much greater than for any other type of cable. We have indicated the

immunity to EMI of shielded-twisted pair to be superior, but this advantage is partially limited by the poor assortment of connectors available and by loose specifications. Twisted lines loosely specified as coaxial lines such as RG108A/U are manufactured to more rigid specifications than the ordinary clan of shielded twisted pair. Currently there is no "twinaxial" connector suitable for flying and multi-conductor connectors must be used with resultant compromises in cable shield terminations, impedance matching, and size the connectors. Nevertheless shielded twisted pair is preferable in low frequency magnetic field environments.

The majority of the work observed for flat cable consisted of multi-conductor custom cables for internal package interconnection. One vendor showed a custom single conductor sandwiched between two flat shields, but this cable is extremely stiff and unwieldy. The other vendor made no shielded cables, but recommended separate shield strips laced to the conductors because of the stiffness problem. This last approach is being used by computer companies, but neither the stiff cable or the laced approach appear very attractive for long cable runs. Neither vendor had any type of long off-the-shelf shielded cable.

A more detailed summary of cable and connector state-of-the-art is presented in the following section.

C. CABLE AND CONNECTOR STATE-OF-THE-ART

Cable which we have already generally classed as round or flat can be further classified in subdivisions. Major subdivisions of all cables are commercial and military. The main differences between these classes are completeness of specifications, quality and quality control. Round wire or cable is further subdivided into hook-up wire, multi-conductor cable, and coaxial cable. Any of these may have varying degrees of shielding except that a coaxial cable is by its nature shielded. Our study is restricted to shielded military cables.

Of the shielded round military cables, we will evaluate coaxial cables and twinaxial cables. Conventional military grade shielded twisted pair are acceptable for many instrumentation systems, but where an extensive amount of pulse transmission is present a tighter degree of control on shielding and twisting is desired for good EMI rejection; thus, the twinaxial is the choice. The same statement regarding single conductor versus coaxial cable is applicable.

We have chosen as representative of the art of the following

Standard 53.5 ohm Coax	RG58/U
Subminiature 50 ohm subminax	RG178B/U

Twisted Pair 78 ohm twinax	RG108A/U
Low Capacity----digital coaxial	21-999

Typical specifications for these cables are tabulated in the table of Figure 1. Some comparisons of these cables can be made just from examining the table.

lowest losses	RG58
lowest capacity	21-999
lightest weight	RG178

Most standard coaxial cable and the RG 108A have polyethylene dielectric which can be replaced by teflon with custom specification whereas most subminiature cables with an RG number already have telfon dielectrics. From this information, one can see that the choice of a cable based upon the tabulated data is a matter of selecting the optimum parameters with a compromise of the rest. Our program goal will be to evaluate various installations in the Addressable Time Division Data System for the best choice(s) based on performance.

The state-of-the-art for flat cables is that there are few, if any "off the reel" types for general usage. Standard specifications are just not in existence particularly for a suitable shielded cable. No evaluation of a flat cable is being performed in this study.

There are several varieties of connectors for coaxial cables; for example, types N, BNC, TCN, and UHF. Types N and TNC and

RG/U Type	O.D.	Jacket Type	Shield	Dielectric MTL	Center Conductor	V.P. %	Cap. Pf	Voltage Rating	Z_o ohms	Wt. lbs 1000 ft	Attenuation db @ 10mHz	Center Cond ohms/ 1000 ft	Connector Series
58	0.195	PVC	TC	0.116P	20 C	65.9	28.5	1900	53.5	27	1.25	10.15	TNC
108A	0.235	PVC	TC	.079P(ea)	2-7/28TC	68	23.5	1000	78	29	2.3	10.15	TWIN
178B	0.075	T(FEP)	S	.034T	7/38 SCW	69.5	28.5	1000	50	6	5.6		Subminex
21-99*				NOT AVAILABLE									----

* Not an RG/U type

Nomenclature:

P	polyethylene
PVC	polyvinyl chloride
T(FEP)	Teflon (FEP)
TC	tinned copper
S	silvered copper
C	copper
SCW	silvered copperweld
dimensions	inches

FIGURE NO. 1

ROUND CABLE SPECIFICATIONS

related versions of connectors are a screw type which have or are being used in space applications. The TNC (threaded coupling) connector is probably the most commonly flown connector because it is the smallest acceptable connector for standard coaxial cables. Subminiature cables use a subminiature connector (subminiax) which is similar to the TNC. The TNC connectors are 50 ohm and subminiature connectors are available in either 50 or 75 ohms to match the variations in cables. In addition to individual coaxial connectors there are some AN type multi-conductor connectors with coaxial pins and receptacles. There are twin connectors similar to type N and BNC. The BNC (bayonet) version is not suitable for space applications and the connector similar to type N is large and has not been tested to space environments. Presumably the BNC version could be converted to a TNC shell, but absolute evaluation is not possible at this moment. Most installations of shielded twisted pair consist of the use of multi-conductor AN connectors such as the Bendix Pygmy version where the two conductors use two pins of the connector and the shield may or may not be carried through the connector by a separate pin. No impedance matching occurs and maximum shielding is compromised, but the installation can be adequate depending on the environment.

All of the above connectors except the twin lead are available with crimp or solder connections. Further description is left to the vendor catalogs. In reference to crimp or solder

connection, there seems to be a majority opinion that good crimp connections are superior to solder joints.

II. OPERATING CHARACTERISTICS OF CABLES WITH PULSE SIGNALS

General transmission line theory is applicable to the analyses of cables with stepped or pulsed voltages. A rigorous solution of a multiple distributed load system such as the Addressable Time Division Data System is extremely difficult especially if cable stubs to the loads are involved. Monthly Progress Report MCR-67-266 (Issue 3) (1) presents good emperical solutions for typical systems. This report is summarized and expanded upon the following paragraphs:

A. SIGNAL REFLECTIONS, THEIR CAUSES AND EFFECTS

Termination of a transmission line in other than its characteristic impedance can result in reflections. If a line is loaded with its characteristic impedance and driven by a signal generator of arbitrary impedance there will be essentially no reflections. If the line is tied with cable stubs to the distributed loads it will be impossible to avoid reflections because no combination of loads can be practically selected to match the transmission line. If the stubs are degenerated to zero length represented by a "looped" cable arrangement where the cable goes from one load to another, high impedance loads along the line will not disturb the signal if characteristic termination is employed at the remote load end of the line. A looped multiplexer system with high input impedance multiplexers can be driven easily by

signal sources with clock rates in the low megacycle region. In fact, the upper limit of clock rate should be only limited by the cable parameters: capacity, line loss, propagation delay, and by the speed of terminating circuits.

There appears to be no significant difference in performance in systems when operated from current sources (high impedance) or a voltage source (low impedance) but there are practical differences which may dictate a choice. A current source must be operated on a higher voltage than that required by the load and is, therefore, less efficient than a voltage source. A current source with its high impedance characteristics may automatically perform the switching or commutating function which would require separate circuits for a voltage source. A voltage source is less critical to possible system shortcomings created by leakage reactances of transformers or inadvertent resonances because the low impedance provides a good damping factor. An example of this occurred during the laboratory tests and will be discussed in Chapter III.

The foregoing statements are not intended to say that telemetry or other pulse systems cannot be operated without termination of the lines in their characteristic impedance. As stated in the third monthly progress report, digital systems with clock rates up to 500kHz can be operated successfully with high impedance terminations. Reflections still exist, but their time

duration are short compared with information periods. The major care that must be taken in the operation of an unmatched system is that the line is loaded adequately to limit the magnitude of voltage steps caused by reflections to a level so that terminating circuits will not misconstrue exterior voltage transitions as clock pulses. The obvious advantage of being able to operate a transmission line with high impedance loading is a reduction in power consumption (% losses are, of course, greater because of reflections).

Up to this point in writing, the effects of reflections have been defined as creating timing errors which can contribute seriously to the malfunction of digital systems. It should be remembered, however, that summations of signals and their reflections will create serious amplitude errors in PAM measurements. These can only be avoided by matching the lines or running a system slow enough to permit the monitoring of data after adequate time has been allowed for the damping of the reflections.

The preceding information is well substantiated by the analyses and laboratory conformation described in Monthly Report Issue 3.[1]

B. THE EFFECTS OF CABLE PARAMETERS

Cable parameters for the most part, contribute to system limitations. If a line is terminated in its characteristic

impedance power consumption is high because most lines have characteristic impedances of 50 to 75 ohms. Voltage source impedance must also be well defined (preferably quite low) or PAM data cannot accurately be monitored because of inaccuracies in determining the voltage division resulting from series combinations of source and load impedances. The insertion loss due to long transmission lines is deleterious when compared with low terminating impedances but insertion losses can contribute to the damping of reflections in a mismatched digital system. This effect was demonstrated during the cable test and further described in Chapter III. A quantitative analysis of damping effects will not be attempted herein as lossy lines complicate ideal transmission line theory.

The propagation time of cables which varies with cable design creates timing delays of about 1.5 nanoseconds/ft (based on 68% propagation velocity). This delay time may not be negligible in high speed systems and more will be said in Chapter IV.

The effects of cable capacity are similar to those of a low pass filter. As the terminating impedance of a line is increased the overall frequency response will be reduced simply because dominant loading of the line is capacitive and stored energy cannot be changed rapidly enough. Therefore, the high frequency components of the transient voltages will be attenuated and digital pulses will appear rounded as seen in the photographs of Chapter III.

III. LABORATORY TESTING OF A SIMULATED ADDRESSABLE TIME DIVISION DATA SYSTEM

Laboratory substantiation of all studies is important in the respect that high confidence in results should be established and practical aspects of a system that may have been overlooked in "paper" analysis can be discovered. A breadboard simulation of the Addressable Time Division Data System was constructed. This breadboard contains a programmer, four multiplexers, power supplies and data sources. Terminal plates containing connectors for various cables were installed for evaluating cable runs of the different cables either as data cables or as address cables.

A. THE BREADBOARD SYSTEM

The cost and time involved in the construction of a full scale programmer, and multiplexers would exceed the total value of the cable study so the breadboard is simplified. The programmer generates only one eight-bit address converted to RZ with eight bit synchronization which is sufficient for proper clock and synchronization detection by the multiplexers. The clock for this programmer is a laboratory pulse generator which allows a very wide frequency range of operation. The multiplexers are each addressed by two bits of the eight bit code but the synch bit actually synchronizes each multiplexer to the proper two bits.

Very simple synch detection circuits and transformer inputs to the address system are employed so that the circuits are actually

more critical to good transmission line performance than the more exotic prototype programmer[2] supplied earlier to NASA (Contract NAS8-20514). Good operation of the breadboard implies excellent performance of the more elaborate units under similar circumstances.

Data isolation amplifiers such as used in the flyable prototype are not used in the breadboard data measuring circuits because we are not concerned with isolation of the low impedance batteries (which serve as transducers) from the data bus. FET's are employed as data switches because relatively inexpensive low impedance devices are available.

Schematic diagrams of the programmer and multiplexers are shown by Figures Nos. 2 and 3 respectively. Figure No. 4 shows the programmer timing diagram, and Figure No. 5 shows the timing at the multiplexers. If the timing diagrams are examined, operation of the system should be self explanatory.

Separate power supplies are used for each of multiplexers and programmers for the maintenance of separate grounds. If common supplies were used data and address cable ground returns would be bypassed by the power supply. A laboratory dual voltage supply is used for operating the programmer. Four power supplies are constructed from filament transformers and a Variac to supply power to the multiplexers.

Figure No. 6 is a block diagram of the entire breadboard

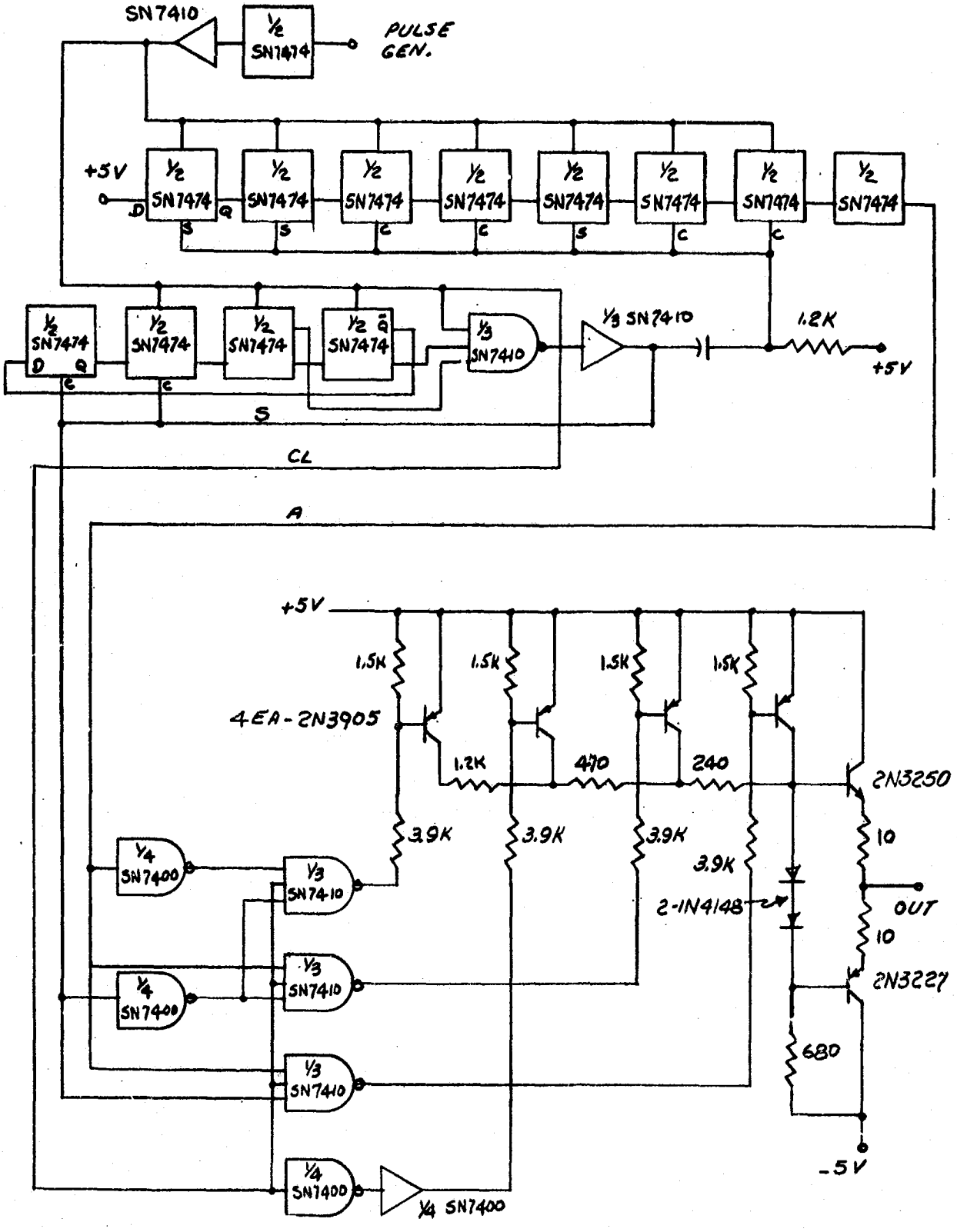


FIGURE NO. 2. BREADBOARD PROGRAMER

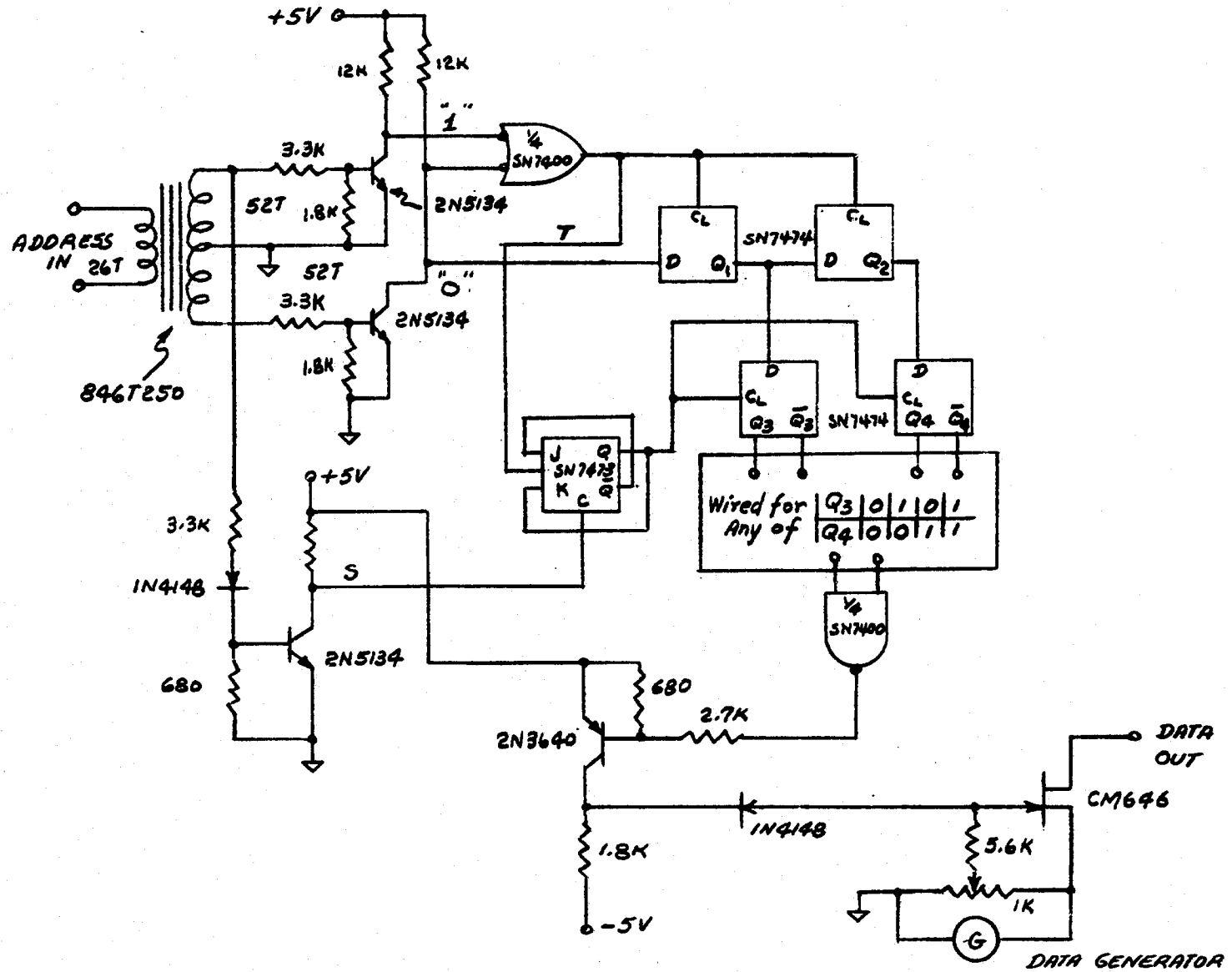


FIGURE NO. 3. BREADBOARD MULTIPLEXER

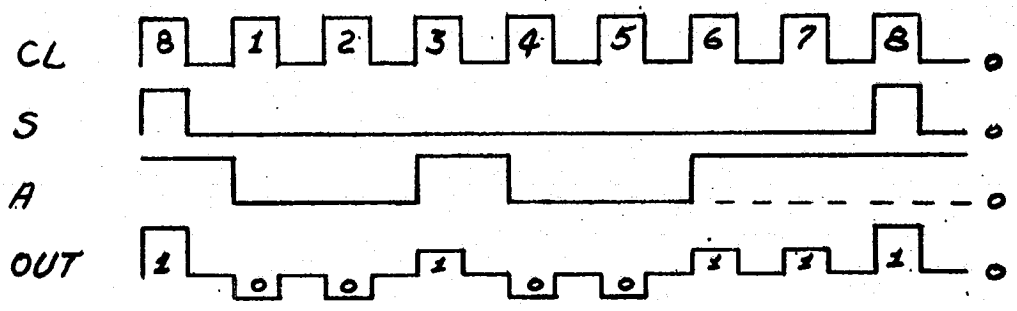


FIGURE NO. 4. PROGRAMER WAVEFORMS

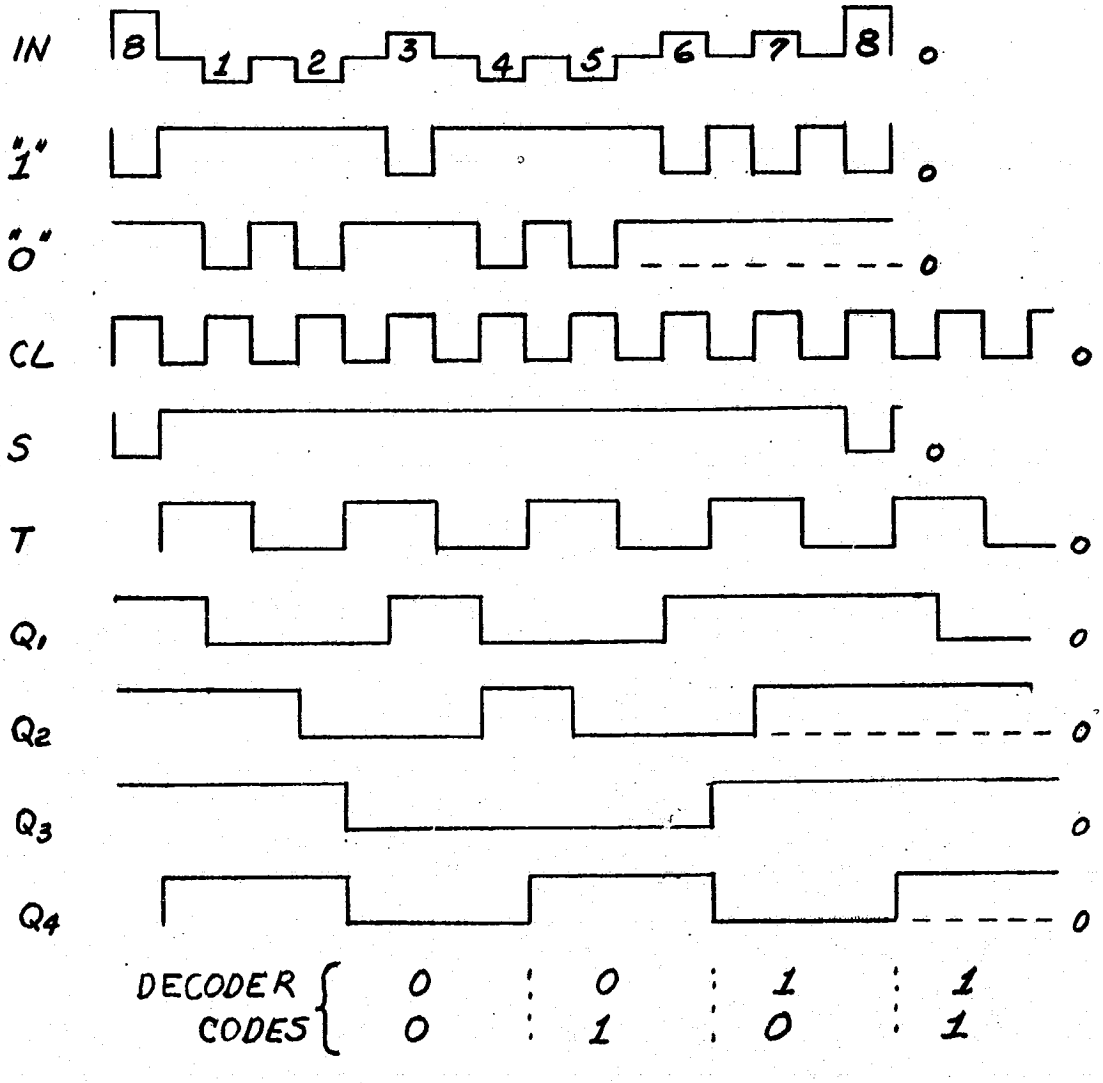


FIGURE NO. 5. MULTIPLEXER WAVEFORMS

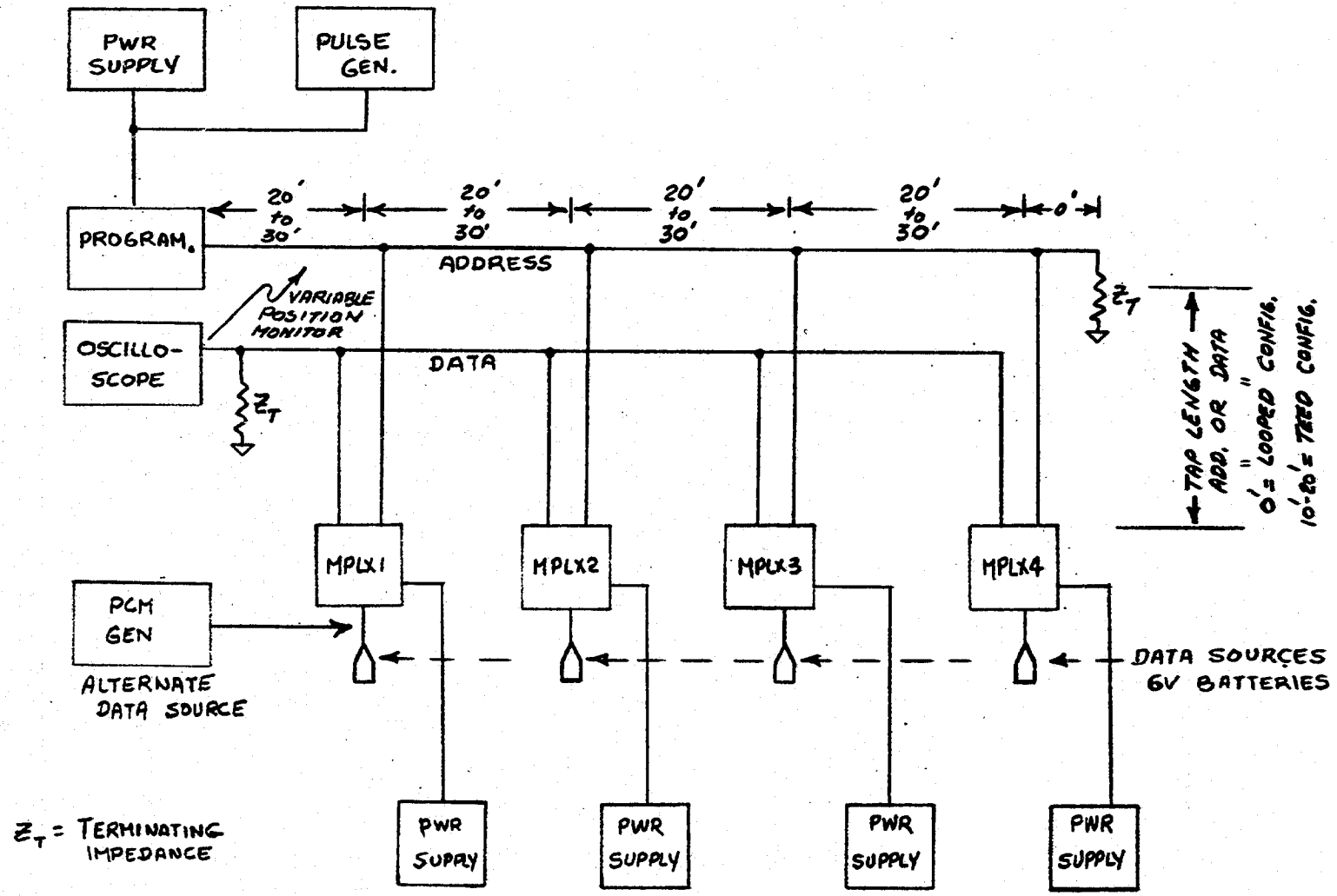


FIGURE NO. 6. BLOCK DIAGRAM BREADBOARD TEST SYSTEM

system and Figure No. 7 is a photograph of the laboratory setup. The address and data buses are about 100 feet long for any cable specimens. The stub sections shown on the diagram are generally degenerated to zero length, (looped system) except for one representative case which will show the difficulties encountered when stubs exist.

B. THE TEST PROCEDURE

The test procedure is to install and evaluate each of the four selected cables (RG 58/U, RG108A/U, RG178B, and Amphenol Cable No. 21-999) in both the address and data bus positions. Factors to be considered are as follows.

1. The effects of terminating impedances upon the maximum operating frequency of the system.
2. The effects of terminating impedance upon the damping time of amplitude distortion due to reflections of PAM.
3. The contribution of transmission line parameters to errors in accuracy measurements of PAM data.
4. The contribution of transmission line parameters to limiting the maximum operating frequency.
5. A comparison of programmer voltage and current drive outputs as related to system operation.
6. An evaluation of shield grounding methods as related to system operation (exclusive of EMI).

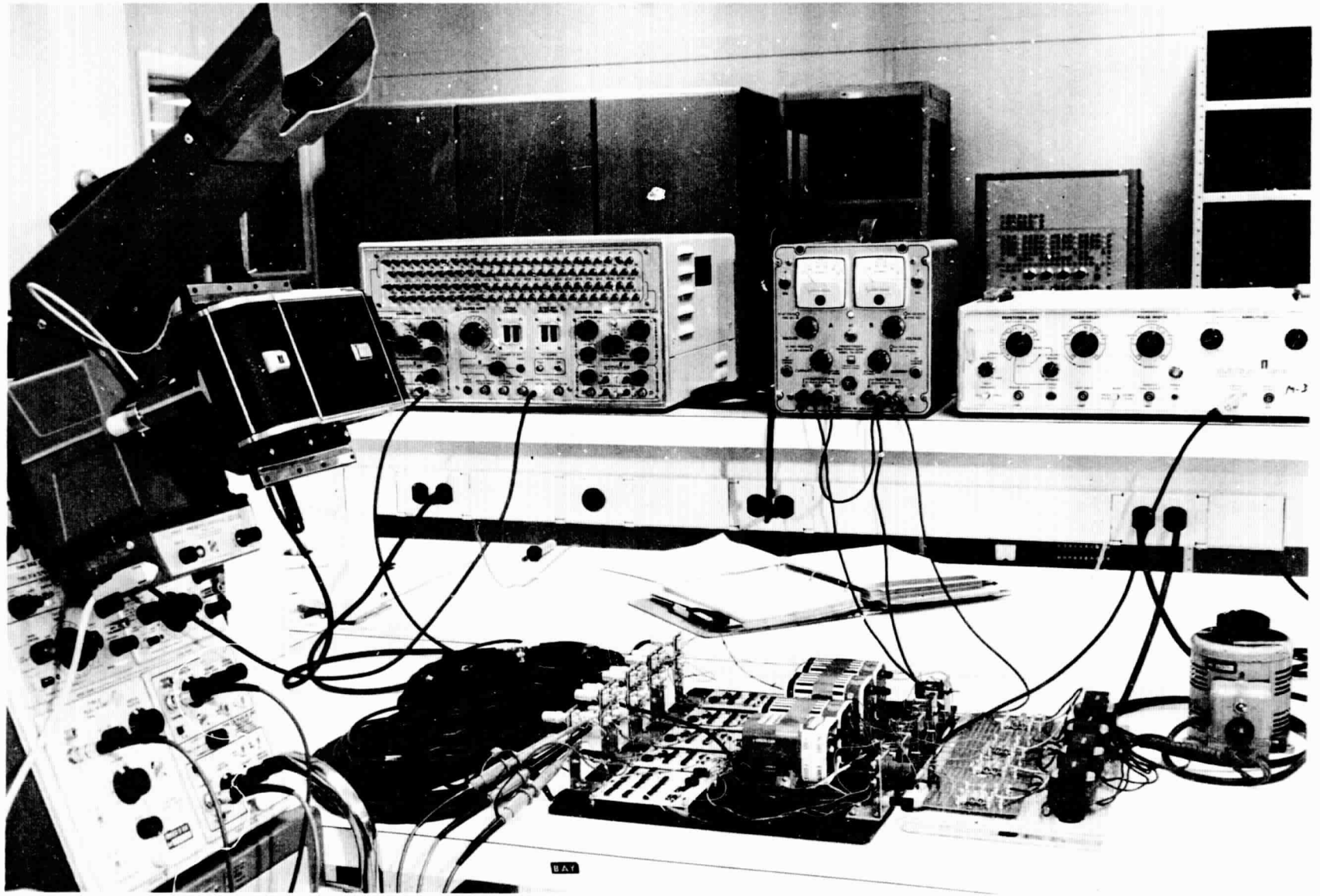


FIGURE NO. 7. LABORATORY TEST SYSTEM

If all of the factors are to be appropriately evaluated, care must be taken in the monitoring of data. An oscilloscope is adequate for instrumentation, but the use of single ended and differential amplifiers must be employed so that the simultaneous monitoring of several data points will not disturb the system either by loading or the creation of false ground paths. This is to say that if the programmer output is monitored by one trace and the address or information of a multiplexer is shown simultaneously the oscilloscope shall not be commonly grounded to both in such a manner as to disturb the normal cable interconnecting paths.

C. CABLE EVALUATION

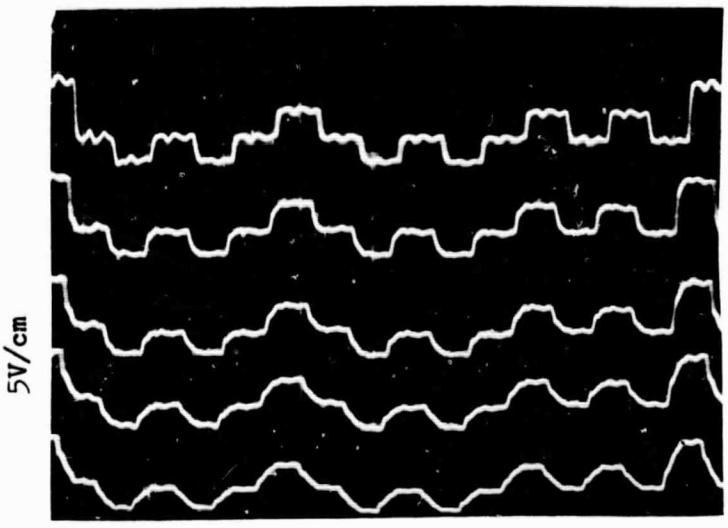
If the effects of cables on the Addressable Time Division Data System are to be seen in their proper perspective, a knowledge of breadboard operation with very short interconnection is necessary. The breadboard as designed was found to operate with clock rates from about 20 kHz to 3 mHz. The programmer is the limiting circuit at the high frequency end and the transformers in the multiplexer determine the low frequency end. It was later determined that the bandwidth of the transformers, which were hand wound, could have been extended by tri-filar winding of the primary and two halves of the secondary. Although toroid cores are used leakage reactance of separately wound coils becomes apparent in pulse applications. Multiple conductor winding is more difficult and cannot be accomplished by some toroid winding machines but is

certainly desirable. In determining the qualities of the data circuits it should be said that the switching rate of the switches used is adequate but the internal resistance of the switches is about 30 ohms which is not truly compatable with 50 ohm termination of lines or line capacities. The foregoing knowledge is adequate for the following comparison of the cables:

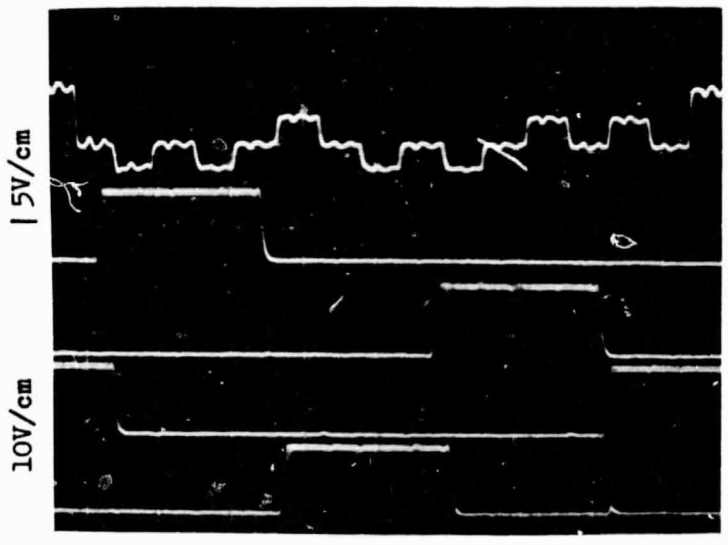
1) Cables as Address Buses

Thirty foot lengths of RG58/U cable were connected between programmer and the first multiplexer and between multiplexers. The "looped" or zero length stub arrangement was constructed and tested first. Then the interconnecting cables were changed to provide 20 ft. lengths between "Tees" with first 10 ft. stubs and then 20 ft. stubs to the multiplexers. The upper photograph of Figure No. 8 shows the programmer waveform for near maximum operating frequency and compares the addresses of each of the multiplexers in the loop system when terminated by 50 ohms. The maximum clock frequency is about 2 mHz. The lower photograph shows correct decode detected pulses time related to the address. Multiplexers 1 through 4 respectively decode addresses consisting of bit pairs 7-8, 3-4, 5-6, and 1-2 throughout the test. The decode pulses should always occur during the two-bit period follow-

Cable runs = 30 ft.



0.5 sec/cm
Address Comparisons
Z_T = 50 ohms



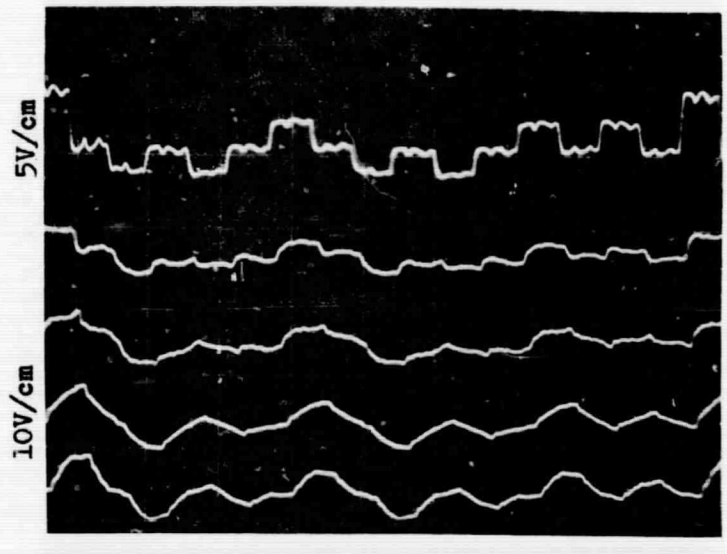
0.5 sec/cm
Decoded Pulse Comparisons
Z_T = 50 ohms

FIGURE NO. 8. PERFORMANCE OF RG58/U CABLE AS "LOOPED" ADDRESS BUS

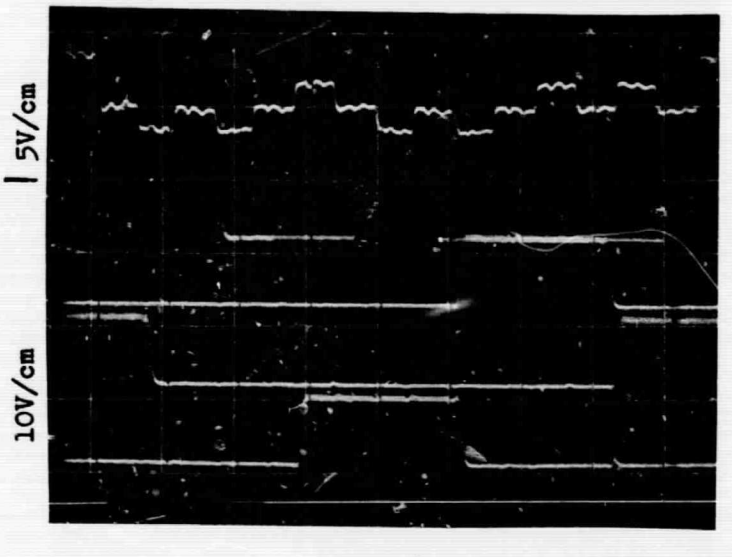
ing the addresses. Figure No. 9 shows addresses and decode pulses for the same configuration, but with a 470 ohm load; note that multiplexer 1 has malfunctioned. Deterioration of the addresses because of reflections is apparent. Figure No. 10 shows the addresses and decode pulses of each of the multiplexers when the main cable is terminated in 50 ohms and each multiplexer is attached with a 10 ft. stub. Multiplexer operation as shown in Figure 10 was satisfactory. The upper half of Figure No. 11 shows the degradation in addresses as the stub length was increased from 10 ft. to 20 feet and the lower half of the figure shows further deterioration of the addresses when the load is changed to 470 ohms. As expected, the system malfunctioned with the last arrangement.

Twenty-five foot lengths of RG108A/U were connected in the "looped" address cable configuration terminated by 82 ohms at multiplexer No. 4. Figure No. 12 compares the addresses and the decode pulses at maximum operating frequency. The comparative pulses are very similar to those shown for the RG58/U cable. Mismatched characteristics which are not illustrated are also similar to those of RG58/U.

Cable runs = 30 ft.



0.5 microsec/cm
Address Comparisons
Z_T = 470 oms

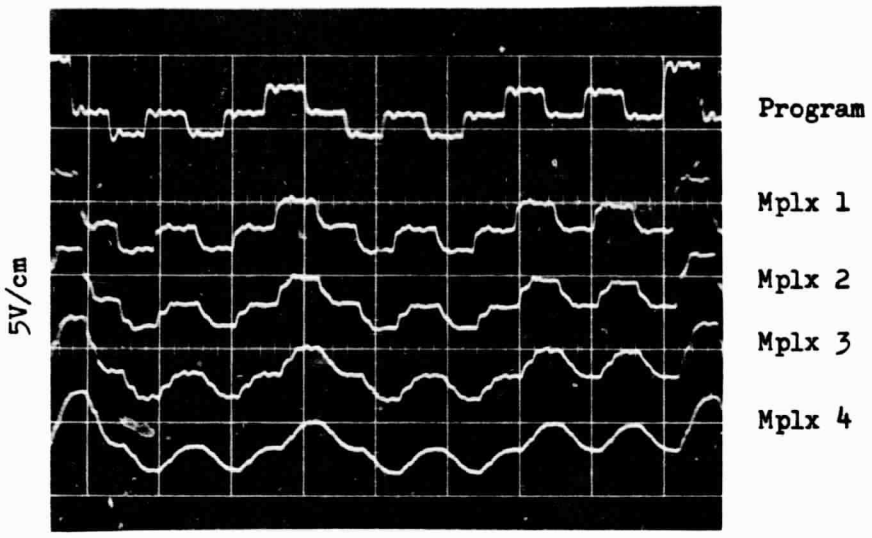


0.5 microsec/cm
Decoded Pulse Comparison

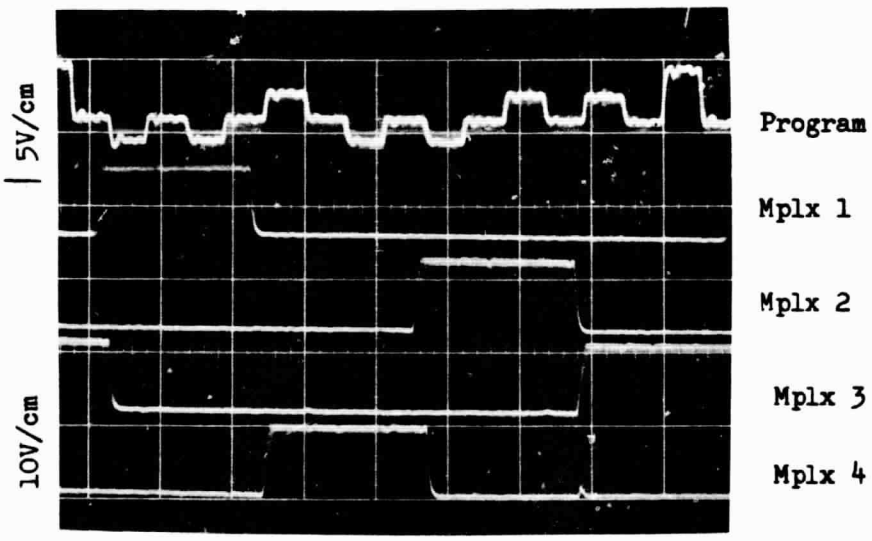
FIGURE NO. 9. PERFORMANCE OF RG58/U CABLE AS "LOOPED" ADDRESS BUS

Cable runs = 20 ft.

Cable tabs = 10 ft.



0.5 microsec/cm
Address Comparisons
Z_T = 50 ohms

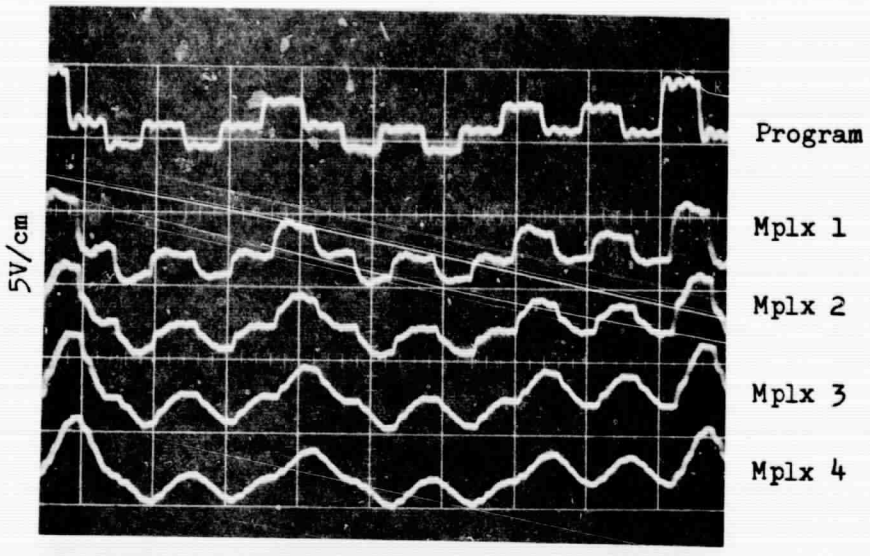


0.5 microsec/cm
Decoded Pulse Comparison

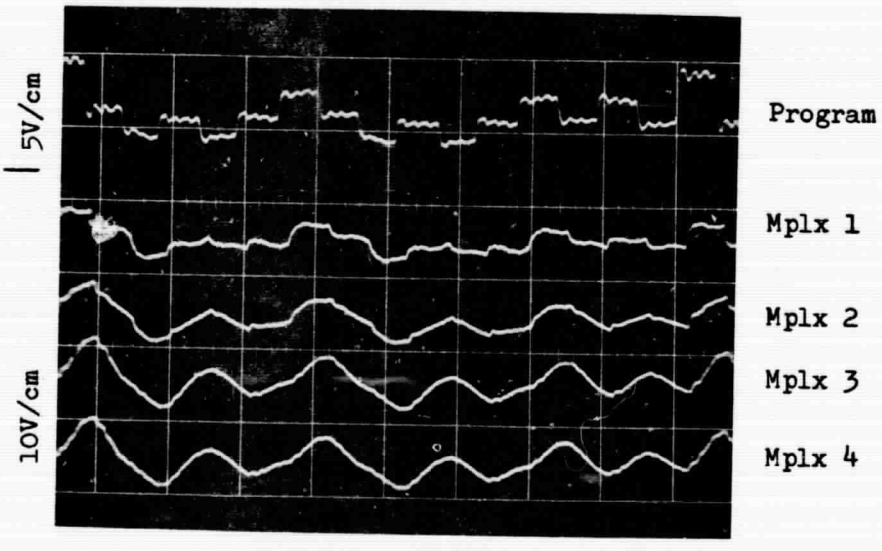
FIGURE NO. 10. PERFORMANCE OF RG58/U CABLE AS "TEED" ADDRESS BUS

Cable runs = 20 ft.

Cable tabs = 20 ft.



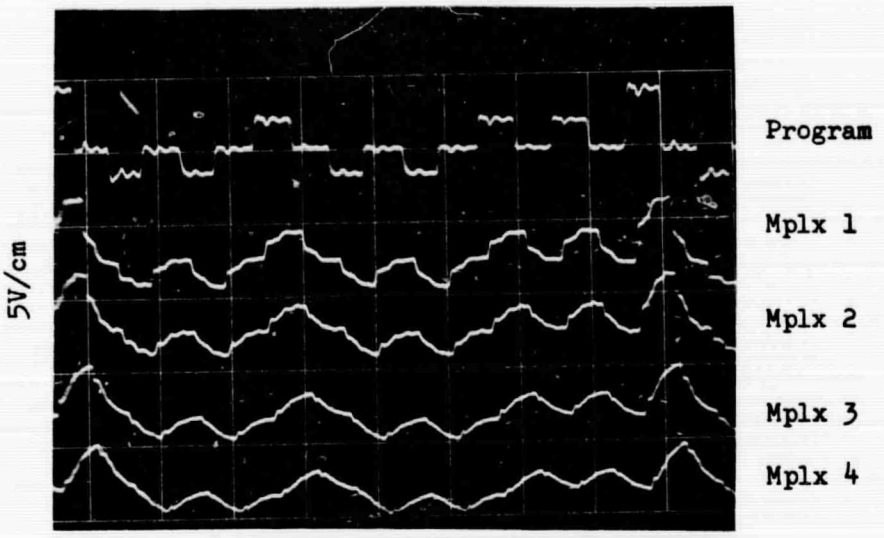
0.5 microsec/cm
Address Comparisons
Z_T = 50 ohms



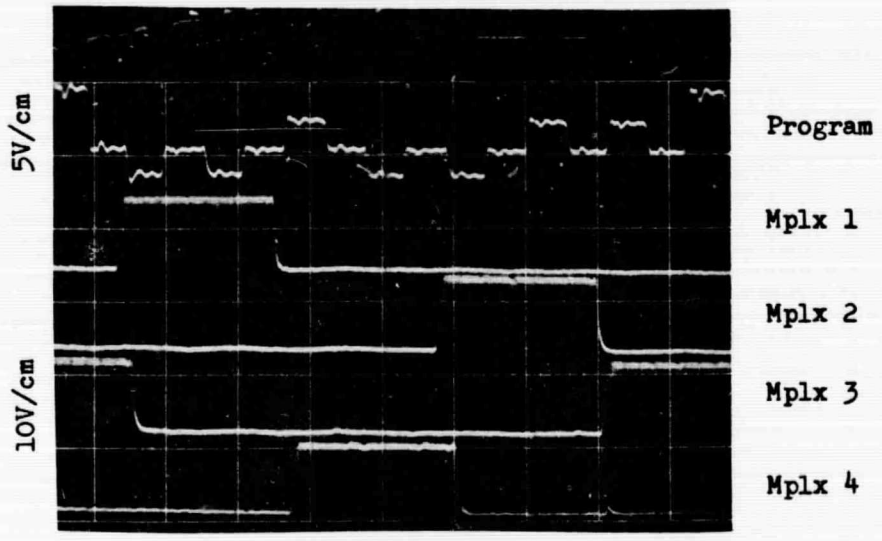
0.5 microsec/cm
Address Comparisons
Z_T = 470 ohms

FIGURE NO. 11. PERFORMANCE RG58/U CABLE AS "TEED" ADDRESS BUS

Cable runs = 25 ft.



0.5 microsec/cm
Address Comparisons
Z_f = 82 ohms



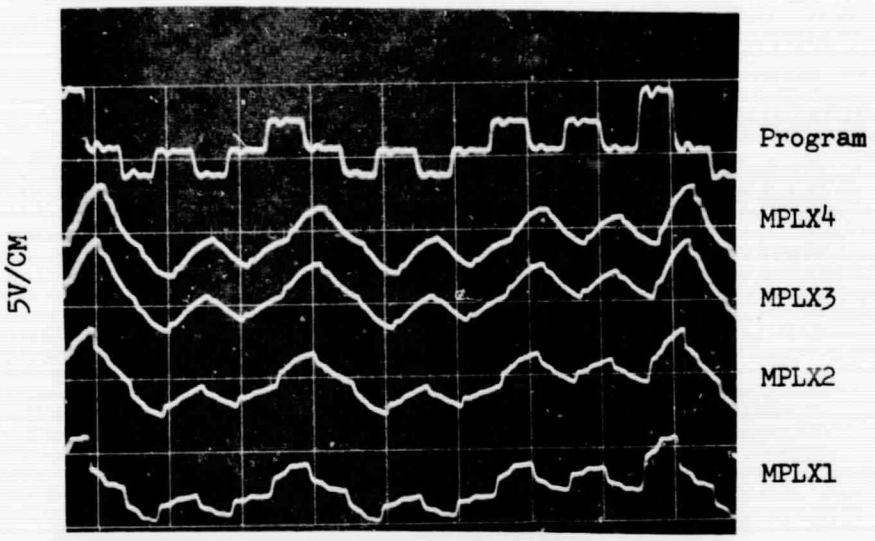
0.5 microsec/cm
Decode Pulse Comparisons

FIGURE NO. 12. PERFORMANCE OF RG108A/U CABLE AS "LOOPED" ADDRESS BUS

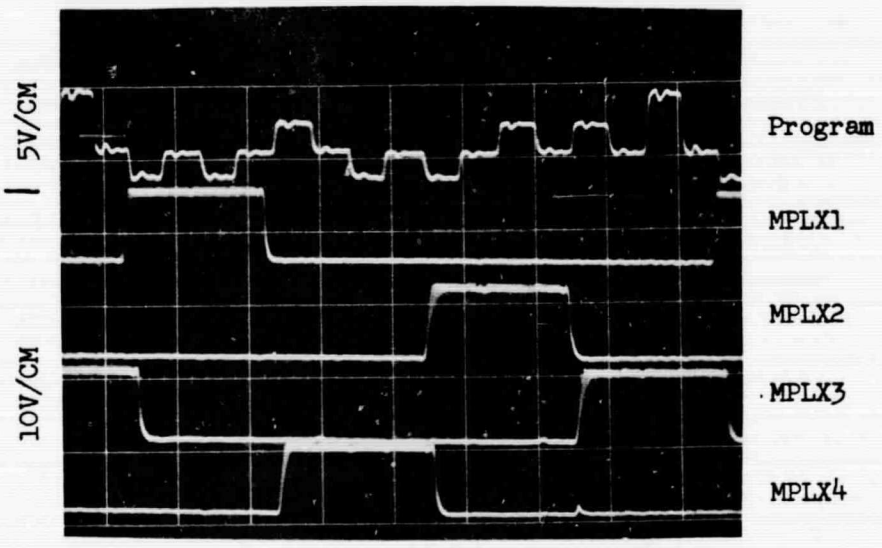
The RG108A/U cable was replaced by an address cable consisting of the No. 21-999 Amphenol digital cable. Exact characteristic impedance of the cable was not available at the time of testing so 82 ohms was left on the line. Operating characteristics were very similar to the proceeding cables and no photographs are included herein.

Operation with the RG178/U cable in "looped" address cable configuration was perceptibly different from the other cables. The system would not work at all with the line terminated in the characteristic impedance. This can be explained by the high resistance of the line which is about 0.23 ohms/ft. With a 100 foot line and a 50 ohm load the voltage of the far multiplexer is only about two-thirds of that generated by the programmer. This high resistance factor seems very disturbing at first but when the system was loaded with 470 ohms operation was slightly superior to all other cables with any termination. The system would run properly at the maximum 3 mHz rate but Figure No. 13 shows correct operation at 2 mHz so that it can be compared with the other illustrations. If the Figure No. 13 photograph is compared with

Cable Runs = 25 Ft.



0.5 Microsec/CM
Address Comparisons
Z_T = 470 Ohms



0.5 Microsec/CM
Decoded Pulse Comparisons

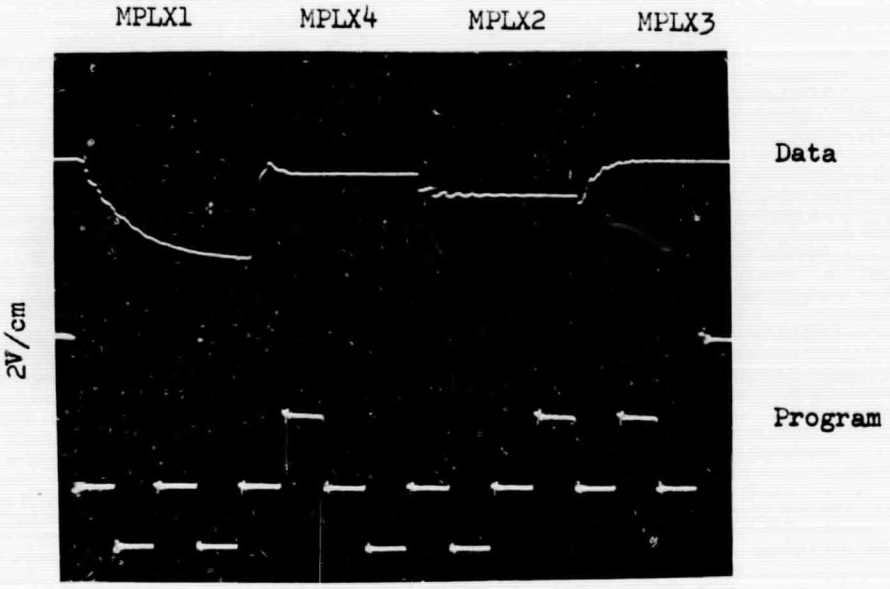
FIGURE NO. 13. PERFORMANCE OF RG178B/U CABLE AS "LOOPED" ADDRESS BUS

Figure No. 9 the distortion of the information when using the RG 178B/U cable load with 470 ohms is clearly less than that for the RG58/U. The most reasonable explanation is that the high line loss of the RG178B/U tends to absorb the reflections to the extent that they are not damaging.

2) Cables as PAM Data Buses

Where cables are used for monitoring PAM data the receiver cannot practically have an impedance to match the line because cable and transmitter losses will contribute measurable errors. While a single signal source presents no serious calibration problem, multiple sources would require individual and tedious calibration for error restrictions of 1% or less. This is primarily due to variable cable lengths offering variable loss between transmitter and detector. The best solution is to design central monitoring circuits with an input impedance as high as practical. Ten times the characteristic impedance of the line is a reasonable evaluating load and all of the lines were tested with this type of loading.

The thirty-foot lengths of RG58/U cable were connected in the "looped" data bus configuration with a 470 ohm termination at the receiver. Figure No. 14 shows



2 Microsec/CM

Data Time Referenced to Address

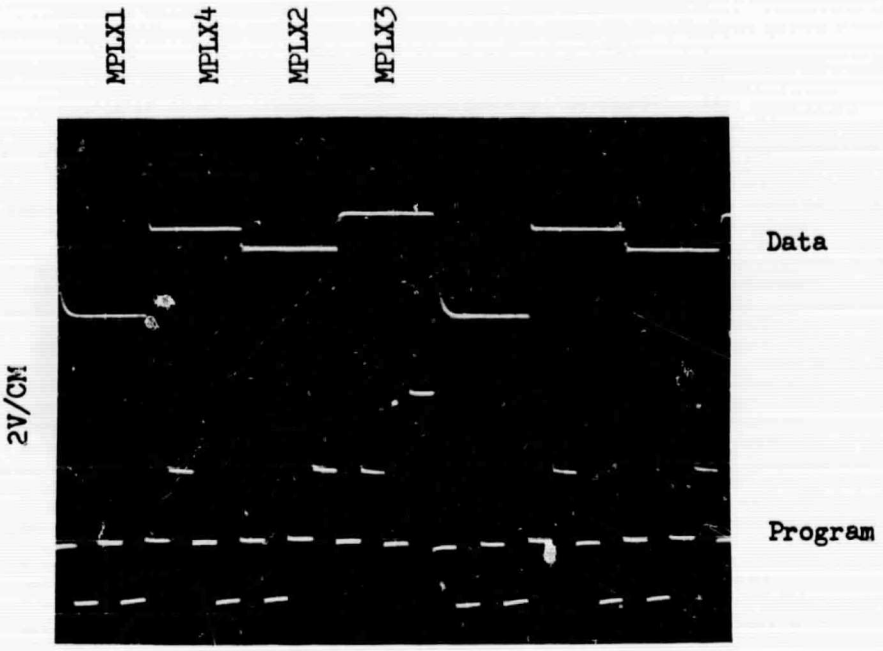
Cable Runs = 30 Ft.

Z_T = 470 Ohms

FIGURE NO. 14. - PERFORMANCE OF RG58/U CABLE AS "LOOPED" DATA BUS
470 OHM TERMINATION

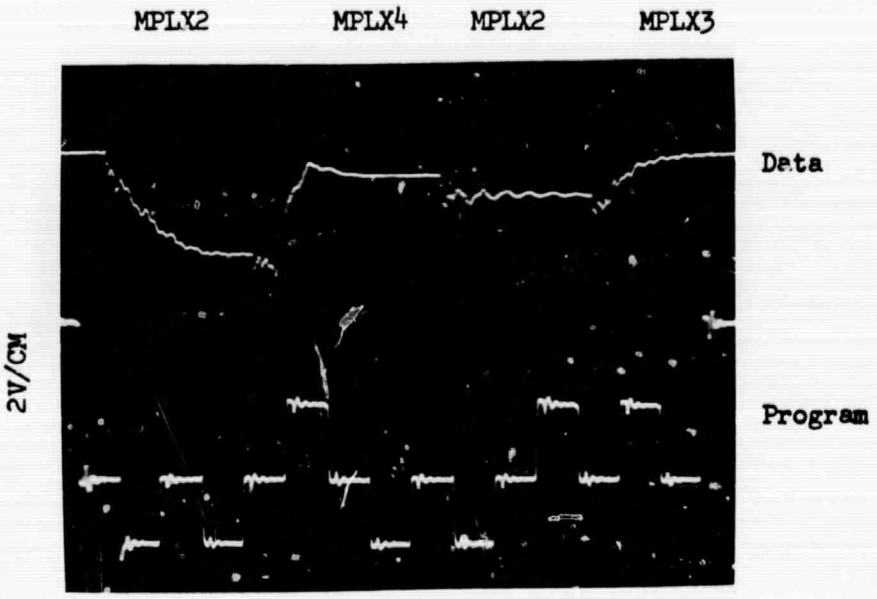
that the data is fairly free of reflections in about 3-microseconds. The data sequence shown on the diagram is MPLX 1, 4, 2 and 3. Data from multiplexer 1 is not shown flat in a 5-microsecond period but this is because that driven end of the line was open. The exponential curve represents the discharge of the stored energy provided by multiplexer 2 into the 470 ohm load (calculated time for 5 time constants = (5)(2850pf)(470 ohm)(10^{-12}) 6.7 μ sec . In all cases the switching times will be less if the data switch impedances approach zero. The apparent time for attenuation of reflections, however, remains nearly constant. Accurate theoretical analysis of the reflections of Figure No. 14 is almost impossible because impedance of the data switches cannot be accurately defined during switching. Figure No. 15 shows sample times of 20 microseconds where the data becomes quite flat.

The RG58/U was next connected in the "teed" configuration with 20 ft. spacing and 10 ft. taps. Figure No. 16 shows considerable degradation of data. Note that some of the reflections are quite perceptable after 4 microseconds.



20 Microsec/CM
Data Time Referenced to Address
Cable Runs = 30 Ft.
Z_T = 470 Ohms

FIGURE NO. 15. PERFORMANCE OF RG58/U CABLE AS "LOOPED" DATA BUS



2 Microsec/CM
Data Time Referenced to Address

Cable Runs = 20 Ft.
Cable Taps = 10 Ft.

Z_T = 470 Ohms

FIGURE NO. 16. PERFORMANCE OF RG58/U CABLE AS "TEED" DATA BUS

The 25-foot lengths of RG108A/U were connected as data buses with an 820 ohm termination at the receiver. Figure No. 17 shows the results. There is not great difference between the data transmitted by RG58/U and RG108A/U although the reflection damping time for the RG108A/U seems slightly shorter.

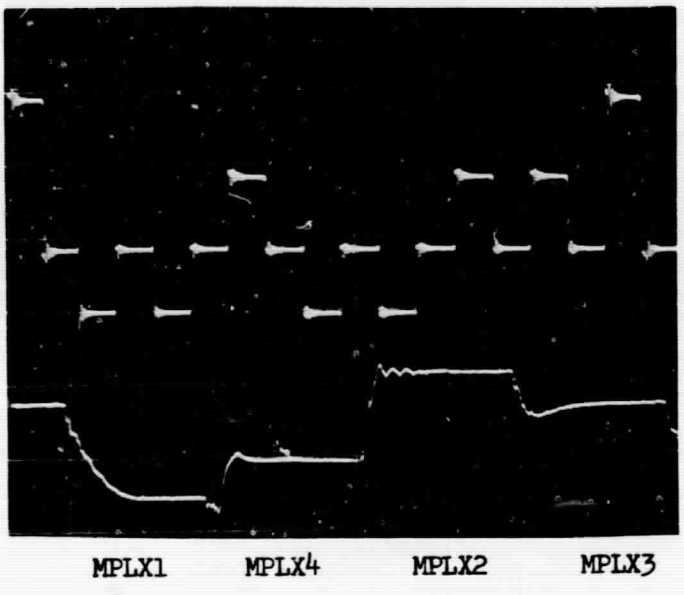
The very good damping characteristics of RG178A/U are illustrated in the analog application shown in Figure No. 18. The line is terminated at the receiver with 470 ohms. Of course, this photograph does not illustrate amplitude inaccuracies due to the high cable resistance.

The digital cable showed no particular advantages over other cables and no data is included herein for the cable as an address cable.

D. VOLTAGE DRIVE VS CURRENT DRIVE

We have had several discussions regarding the relative merits of current drive versus voltage drives both for digital and analog data. Voltage drive implies a low impedance source where the power output efficiency of the driver is high. A current drive is a high impedance source where the current can be proportional to an input drive signal. Repeating an earlier statement, this driver will be less efficient for an equal voltage across the

2 Microsec/CM



Data Time Referenced To Address

Cable Runs = 25 Ft.

Z_T = 820 Ohms

FIGURE NO. 17. PERFORMANCE OF RG108A CABLE AS "LOOPED" DATA BUS

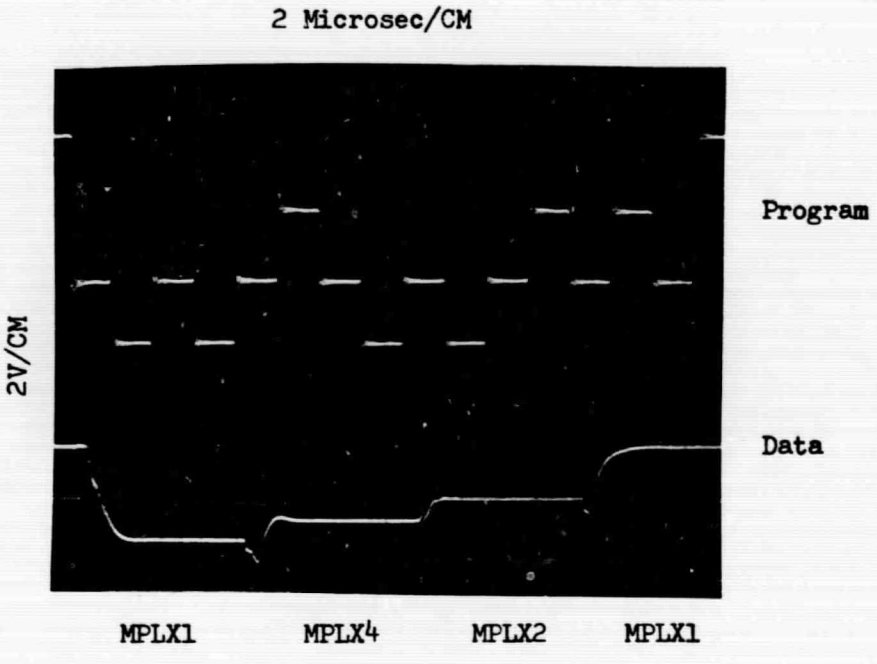


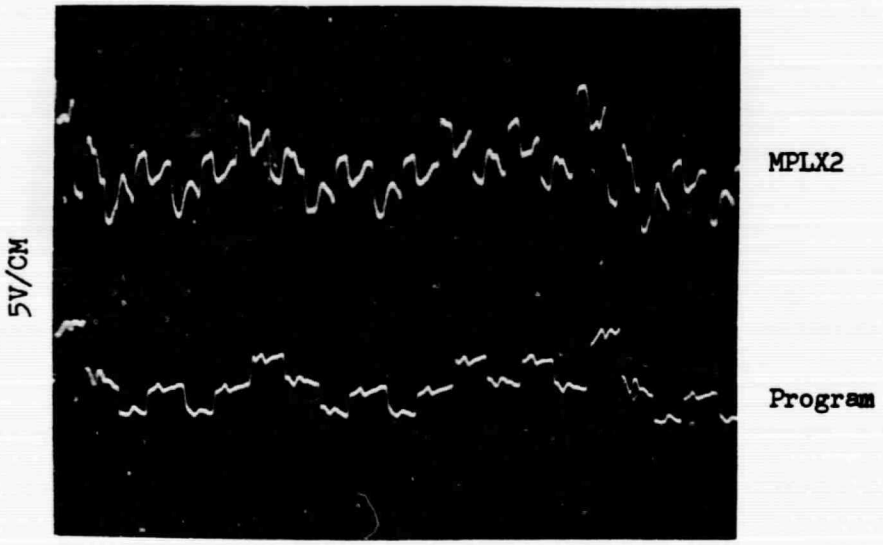
FIGURE NO. 18. PERFORMANCE OF RG178B/U CABLE AS "LOOPED" DATA BUS

load (compared with voltage source). The current driver has an advantage over a voltage source, in that a current source can be its own line switch. Other characteristics seem similar but discussions never entirely resolved this fact in all minds, so laboratory testing was proposed.

RG108A/U cable was used as an address cable with the output of the programmer converted to about a 50 ma current source. The system did not function correctly even though various current arrangements were tried. Figure No. 19 shows a very distorted address at the output of the driver and not a good waveform at multiplexer No. 2. None of this operation seemed logical so all multiplexer loads were removed and the line just terminated with a resistive load. All waveforms appeared much better as shown by Figure No. 20.

Since the calculated impedance of the multiplexers appear high one must believe that the transformers are deficient. Consequently, commercial transformers were substituted at each point. The results shown by Figure No. 21 are good. The only apparent discrepancies in transformers was believed to have been in leakage resistance, so one of the multiplexer transformers was rewound tri-filar and reconnected to the line. This change resulted in as good performance as was given by the commercial unit.

A very general comparative statement may be made regarding voltage versus current drive which is that, circuits which may



0.5 Microsec/CM

Address Comparison

Cable Runs = 25 Ft.

Z_T = 82 Ohms

FIGURE NO. 19. 50/100 MA CURRENT DRIVE OF RG108A/U "LOOPED" ADDRESS BUS

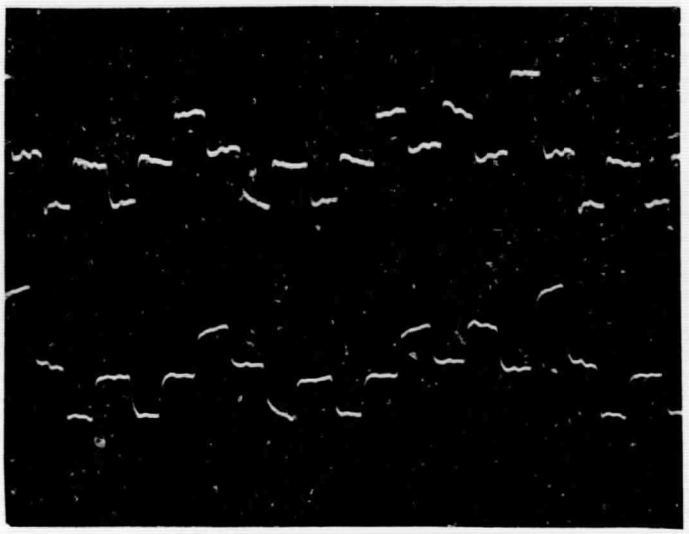
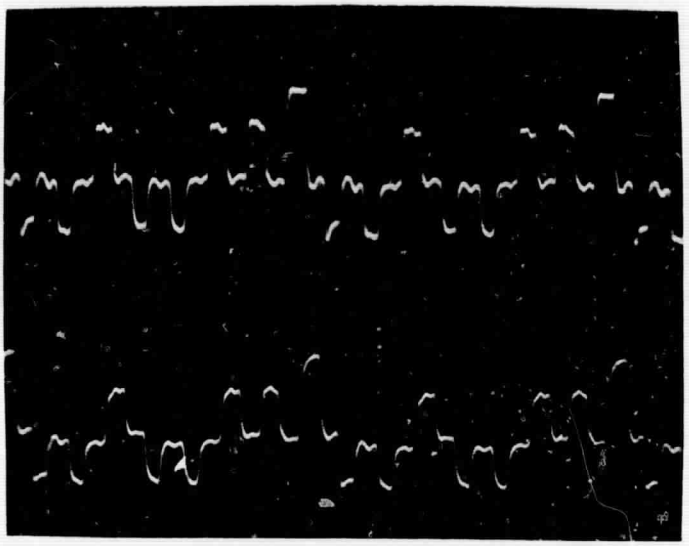


FIGURE NO. 20. PERFORMANCE OF CURRENT DRIVE CONNECTED DIRECTLY TO RESISTIVE LOAD



0.5 Microsec/CM

Address Comparison

NOTE: Aladdin #72-120 6709 Transformers loaded with 2700 Ohms were connected at MPLX1, MPLX2, MPLX4. MPLX3 was unloaded.

Cable Runs = 25 Ft.

Z_T = 82 Ohms

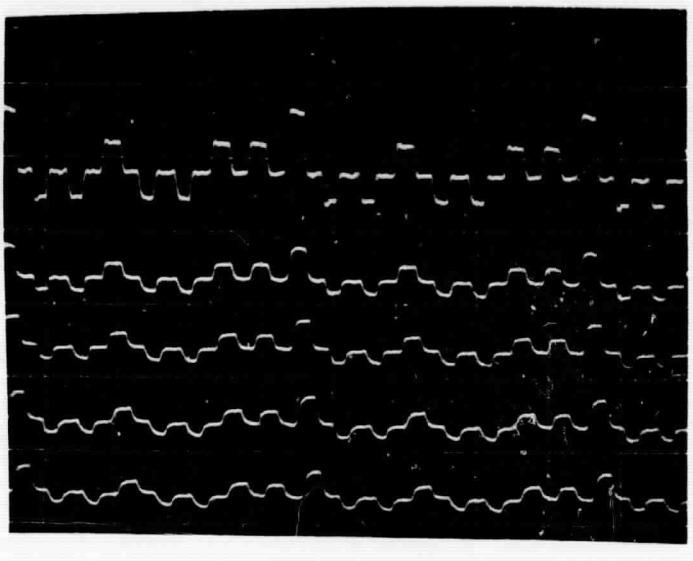
FIGURE NO. 21. CURRENT DRIVE OF RG108A/U CABLE AS LOOPED ADDRESS BUS COMMERCIAL TRANSFORMER LOADS

contain reactive elements resonant at some frequencies may be driven by voltage sources as was done for the majority of these tests. However, if good transformers are employed the choice of drive may be a matter of personal preference. To confirm this, let us show Figure No. 22 which is the voltage drive comparison of addresses at all multiplexer positions with multiplexers removed. While these waveforms are still superior to the current drive waveforms the significance is small.

E. CRITIQUE OF TEST RESULTS AND RECOMMENDATIONS FOR CABLE SELECTIONS

We do not claim that our study of the cable types in operating the Addressable Time Division Data System are exhaustive tests for all representative cables. We do feel, however, that all results conform to general transmission line theory and are representative of all cables with similar characteristics. The tests do point out the limitations that the various cable parameters impose upon system designs, and, as a secondary consideration, some recommendations can be evolved concerning the design and use of coupling transformers for address and data coupling.

The original goals of this study are to make recommendations for the selection of cables and connectors based upon maximum reliability, minimum weight, minimum size, and optimum performance. Our study shows that there is no single cable that accomplishes all of the optimum requirements for a given application.



0.5 Microsec/CM

Address Comparisons

Cable Runs = 25 Ft.

Z_T = 82 Ohms

FIGURE NO. 22. - VOLTAGE DRIVE OF RG108A/U CABLE AS ADDRESS BUS MULTIPLEXERS REMOVED

If all information is digital (address and data) subminiature coaxial cables are the best choice if low frequency EMI levels are low. Except for the general considerations discussed earlier in the report we cannot well define the EMI limitation without testing. The subminiature cable is the lightest, there are numerous flight-proven TNC type subminax connectors available, and circuit operation is excellent. Since the cable is lossy it provides some damping of reflections and higher frequency operation is possible with less loading than is required for other lines. It may be stressed again that the greatest advantage of being able to use a high impedance termination is that system power requirements are less than for a matched line. This is not to say that the unloaded cable is the most efficient because maximum power transfer does occur when the line is matched. Circuit designs must consider resultant voltage drops because of the line losses but the high impedance loads help to minimize these difficulties also. If the information to be transmitted is analog (PAM) the subminiature cable is not especially attractive because, as mentioned before, the variable cable loss from different transmitters makes accurate amplitude detection very difficult.

The preferred cable from an operational standpoint is a shielded twisted pair. Common mode noise rejection is good, cable losses relatively low and ground isolations can be accomplished. Disadvantages are weight and poor connector choices.

Multiple conductor AN type connectors provide the best mechanical terminations but are bulky for single cable applications as well as contributing some discontinuity to shielding. TNC connectors with twin lead inserts would provide good electrical features but the twin lead pints and socket arrangements appear fragile and would be subject to installation damage. No doubt a good connector can be developed but the none seem to exist.

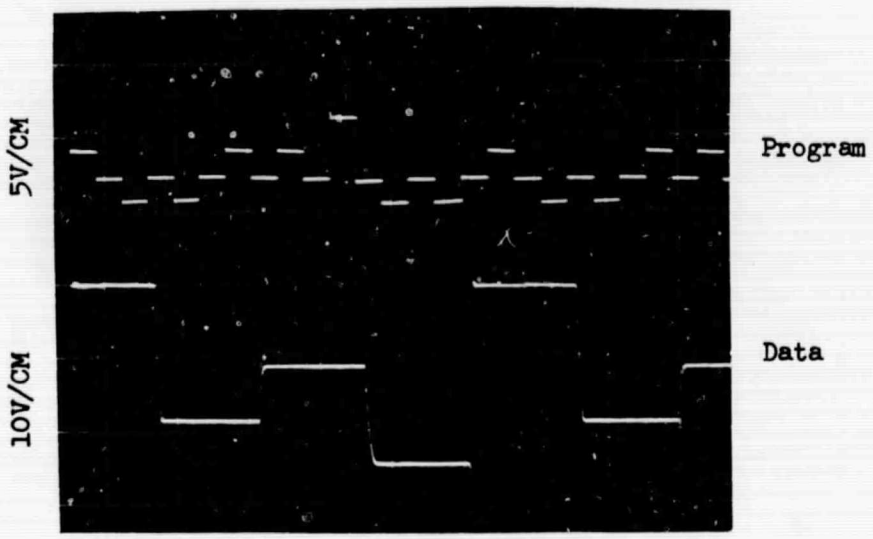
If terminating circuits are designed to avoid ground loops and ground currents can be otherwise avoided and low frequency EMI is not prevalent, the best PAM cable appears to be a conventional coaxial cable. Weight is moderate, connectors are plentiful, and operation is good.

A practical multiplexer system may be constructed with all cable terminated at one end with about 10 times the characteristic impedance of the cable. It is desirable that all multiplexers have much higher impedance than this, say about 100 times the characteristic impedance. While the "looped" cable arrangement is definitely superior to a "teed" cable arrangement, multiplexers can be connected to the main cables by 10 to 20-feed stubs for operating frequencies below about 1-megacycle. No loading of the "teed" system is required other than 10 times the characteristic impedance of the line loaded at the most remote receiver. If any data rates exist above 1 mHz the "looped" system is always recommended. If rates are above about 5 mHz the cables should have

matched terminations regardless of cable type. Recognized grounding procedures shall be followed and modified by experimentation if necessary. One very important procedure was observed in our testing of shielded twisted pair and that was: ground the shield at every multiplexer for the lowest noise. No distinct differences were observed for grounding of coaxial shields.

Optimum reliable applications of the cable are mostly independent of the cable selection (with the exception of comments concerning connectors). Recommendation for usage of redundant cables, redundant circuits, and redundant systems are presented in Chapters V and VI.

The possibility of using transformers for cable couplings and to provide ground isolation and common mode signal rejection have already been mentioned herein and in the monthly progress reports. Testing in this program illustrated acceptable high frequency operation of such transformers even though their leakage reactance was high while Figure No. 23 shows the breadboard system operating at a slow clock rate of about 70 kHz as compared with test rates of 2 mHz. Our experience with the improvement in coupling by multi-filar windings even on toroids indicates that transformers can be wound to work at lower frequencies and yet retain realtively good characteristics in the low mHz region. Contributing further to good coupling is the use of the smallest possible core which will accept the number of turns required for the lowest frequency



20 Microsec/CM

Data Time Referenced to Address

FIGURE NO. 23. - SLOW SPEED PERFORMANCE OF MULTIPLEXER SYSTEM

of operation considered. We can generally suggest that operational amplifiers may be replaced by transformers in many broadband pulse applications where the amplifier is not paramount for impedance matching. The transformer networks will be less complex, less costly, and smaller or at least compatible in size with the replaced circuitry. Common mode rejection of a good transformer can be higher than an integrated circuit amplifier.

IV. SYNCHRONIZATION

Data acquisition systems or parts thereof such as the Addressable Time Division Data System require methods of correlating addresses from the central unit to the multiplexer decoders and commutated return data. Cables with their inherent delays and reflections due to mismatched terminations contribute some problems to synchronization but the following paragraphs will explain that synchronization of a practical system operating in the kHz to low mHz should not be difficult.

A. ADDRESS SYNCHRONIZATION

Synchronization of an address to a multiplexer decoder involves no more than being able to identify which is the start and which is the end of a programmed address. In the Addressable Time Division Data System we have chosen to identify the last bit of an address by a double amplitude pulse. Earlier studies indicated that this technique gives one of the more efficient and reliable systems of synchronization and we have no reason to change this philosophy. There are other methods of synchronization such as sync codes, double width pulses, and phase reversals but none of these studied seems as readily implemented as the double amplitude pulse. In addition to word or address synchronization it is desirable to have synchronization of the individual bits within a multiplexer. Asynchronous loading of addresses into a multiplexer

is possible but problems involved in clocking resultant data weigh heavily in the favor of an entirely clocked system. Individual bit synchronization can be achieved by distributing the central programmer clock around the system via a separate clock line, by synchronizing a free running clock in each multiplexer to the address, or by deriving the clock from the address data. Dervation of the clock is simple, provides positive data synchronization, and saves one cable if an unambiguous waveform is used such as the bi-polar RZ form used in the Addressable Time Division Data System. Cable delays have no effects upon proper decoding of the various multiplexers and reflections are only harmful where they are large enough to be erroneously detected as address bits.

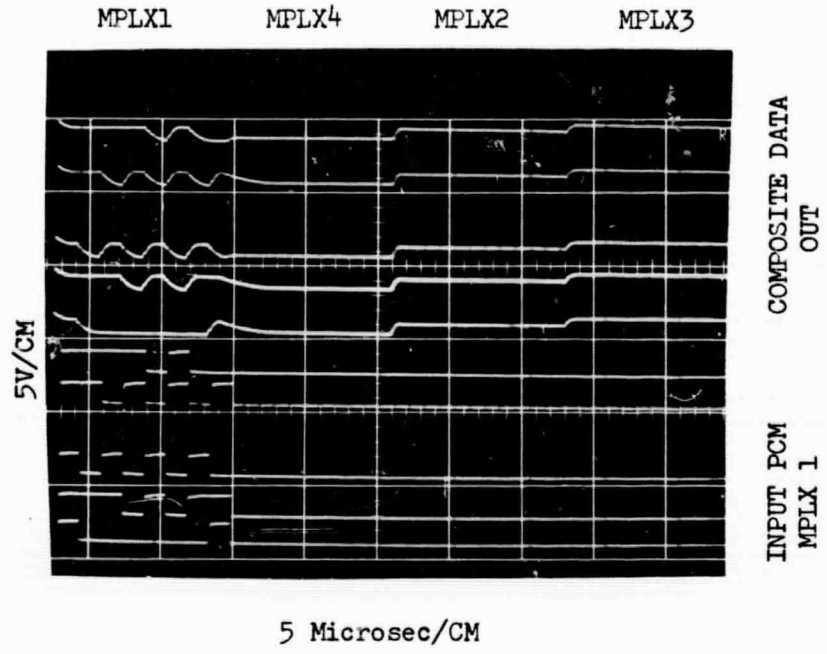
B. DATA SYNCHRONIZATION

Almost all of the synchronization problems in a distributed multiplexer system occur in the recovery of monitored data. Line delays and reflection delays can contribute to the acquisition of wrong data. If clock periods are long, when compared with delay periods, variable delays of data return from the individual multiplexers can be discounted and the data of each multiplexer can be timed out by its own clock as derived from the address with no particular problems. PAM data can be sampled from near the middle of a pulse by employing a fixed delay at the A-to-D converter. PCM data clocked by the derived clocks of a slow system can be monitored by a central processor without special regard to the

relative delays also. Use of the central processor clock may at most only result in neglible shortening of the data pulses.

PCM data can also be sampled where a clock in the A-to-D converter is only synchronized to the appropriate decoded address. The only real restrictions on this technique are that the A-to-D converter clock must be fast enough for the full conversion to occur in the allowed sample time, and the form of PCM data transmission must be acceptable for reconstruction of the data clock at the receiver. An RZ wave form or any of several types of NRZ codes provide information for positive recovery of such a clock. Of course, a clock line may interconnect all of the multiplexers with the central processor for the purpose of transmitting the individual A-to-D converter clocks back to the central unit for data input clocking. Figure No. 24 shows the multiplexed data of the breadboard with PCM data multiplexed by the first multiplexer. The figure illustrates proper synchronization of all eight-bit codes within the sample period. Let it be emphasized here that this asynchronous data would have to be transmitted back either in a form which allows clock derivation or in conjunction with a clock on another line. Otherwise, positive identification of the data is not always possible.

If PCM data is to occur at a high frequency where a bit time is close to the maximum delay time of the system, the looped data bus we have shown will be difficult or impossible to use. If,



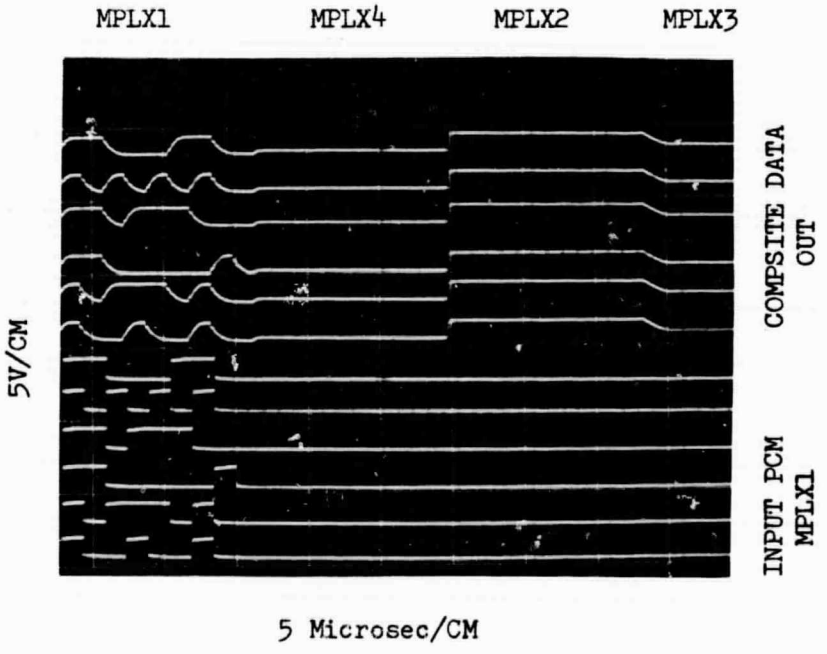
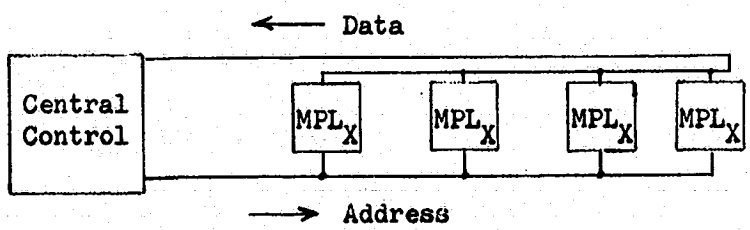


FIGURE NO. 24. - SYNCHRONIZATION AND MONITORING OF PCM AND ANALOG DATA

however, the multiplexers are connected with the address sequence 1,2,3,4 (relative distance from the control unit) and the data return sequence 4,3,2,1, all data is returned to the central unit with approximately the same delay and the delay time is of little consequence in the performance of the system. Such a system connection, which was first described in monthly progress report No. 4, is shown below.



V. ADDRESSABLE DATA SYSTEM RELIABILITY

The four most feasible system configurations developed in the termination and synchronization study have been analyzed to determine their relative reliability. These configurations, shown in Figure V-1, are briefly described below. Each configuration has one central control unit, CCU, and 4 thirty-two channel remote measuring sources, RMS, for a system capacity of 128 channels. Configuration IA has been chosen as the basic configuration since it has one address cable and one data cable. IB is the same as IA except the "loop" configuration provides identical delay between any address and the corresponding data. Since the part count is the same as IA, the reliability is the same. Configuration II has redundant address and redundant data cables. Some additional circuitry is necessary in both the CCU and RMS's. Configuration III uses two cables with addresses and data time multiplexed on each cable to provide cable redundancy using a minimum number of cables. This configuration requires a modest increase in circuitry of the CCU and considerable changes in the RMS's A/D converters. This also doubles the address bit rate and a little more than doubles the returned data rate.

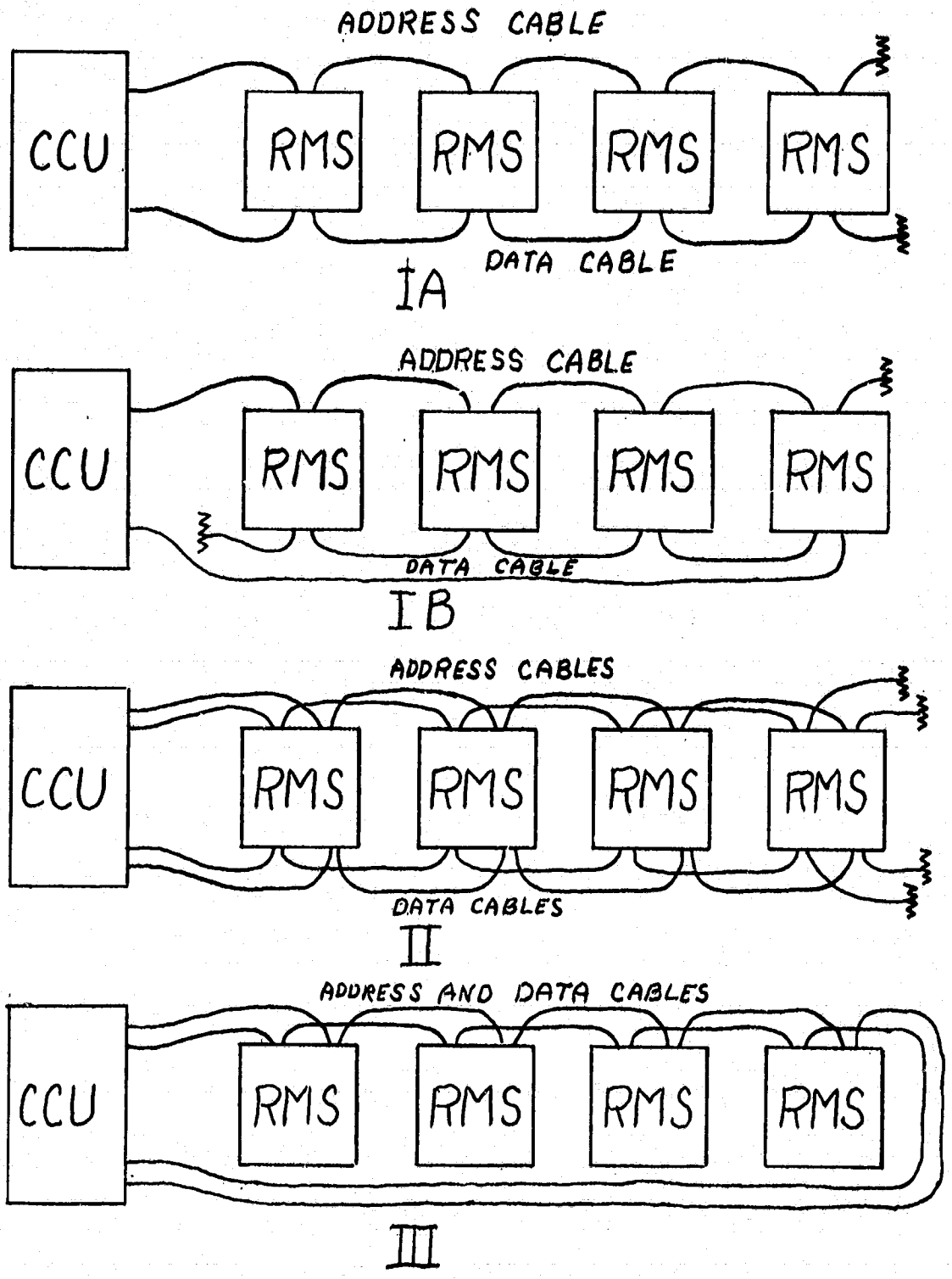


FIGURE V-1

CONFIGURATIONS

The advantages and disadvantages of each configuration are:

Configuration I

Advantages - Minimum complexity

Minimum weight

Disadvantages - Highest failure rate

Configuration II

Advantages - Medium complexity

Redundant cables

Lowest failure rate

Disadvantages - Highest number of cables

Configuration III

Advantages - Medium failure rate

Low cable number

Redundant cable operation

Disadvantages - Complexity

Double bit rate

Since the analyses are only comparative, no environmental or time factors were used in the calculations. Thus the most reliable system is the one having the lowest failure rate. Table V-1 shows the calculated failure rates for the four configurations and the four cases considered for each. The actual calculations are contained in the appendix. These numbers are considerably smaller than those obtained previously due to more

extensive use of integrated circuits and lower failure rates for the piece parts. Table V-2 gives the generic failure rates, G_{FR}, and the application factors, K_A, used in the calculations. These are Voyager numbers and resulted from a consensus of the associated contractors.

TABLE V-1

FAILURE RATES PER MILLION HOURS

Configuration	Case		
	1	2 & 3	4
IA & IB	31.38814	22.57054	3.94798
II	30.34814	21.53058	3.36302
III	30.63644	21.81924	3.70156

The four cases investigated are based on different failure definitions as follows:

Case 1 - Loss of any channel

Case 2 - Loss of two channels

Case 3 - Loss of all data from one RMS

Case 4 - Loss of all data from all RMS's

Table V-1 shows the same failure rates for Cases 2 and 3 because they differ only in the eighth or ninth significant figure.

TABLE V-2

FAILURE RATES, G_{FR}, AND APPLICATION FACTORS, K_A

Component	$G_{FR}(10)^{-6}$ Total	Short	Open	% of Rating	K_A
CAPACITOR, Ceramic or Porcelain	.004			10	.22
				20	.6
				50	2.7
				70	7
CAPACITOR, Tantalum	.02			20	2.9
				60	3.8
				100	5
CONNECTOR, Static per pin	.0001	.00005	.00005	2 pin	1.4
				36 pin	16
CRYSTAL	.01				1
DIODE	.006	.004	.002	10	.1
INTEGRATED CIRCUIT	.02	.013	.007		1
JOINT, Soldered	.0001				1
JOINT, Welded	Assumed in component failure rate				
POTENTIOMETER, Composition	.004			10	1.8
RESISTOR, Metal Film	.003	.0003	.0027	10	.94
				30	1.5
TRANSISTOR, Silicon	.01	.007	.003	10	.07
				25	.1
TRANSISTOR, Field Effect	.02	.013	.007	10	.07
P.C. Board	.01				1

A functional description of the system is given below using configuration I as the base. The other configurations perform the same functions in a slightly different manner. The appendix contains a more detailed description of all configurations.

The CCU provides system synchronization, generates and transmits the address sequence to the RMS's, accepts data from the RMS's and transmits the data to the transmitter modulator. As shown in the block diagram, Figure V-2, the configuration I CCU consists of a clock, an address generator, a PCM output register and driver, and a power supply.

The address generator supplies 7200 10-bit serial addresses per second with address groups occurring as shown in Table V-3.

TABLE V-3

ADDRESS REPETITION RATES

No. of Addresses	Address Type	No. Times Repeated Per Second	Time Slots per Second
6	SYNC	120	220
34	Data	120	4080
54	Data	40	2160
10	Data	12	120
30	Data	4	120

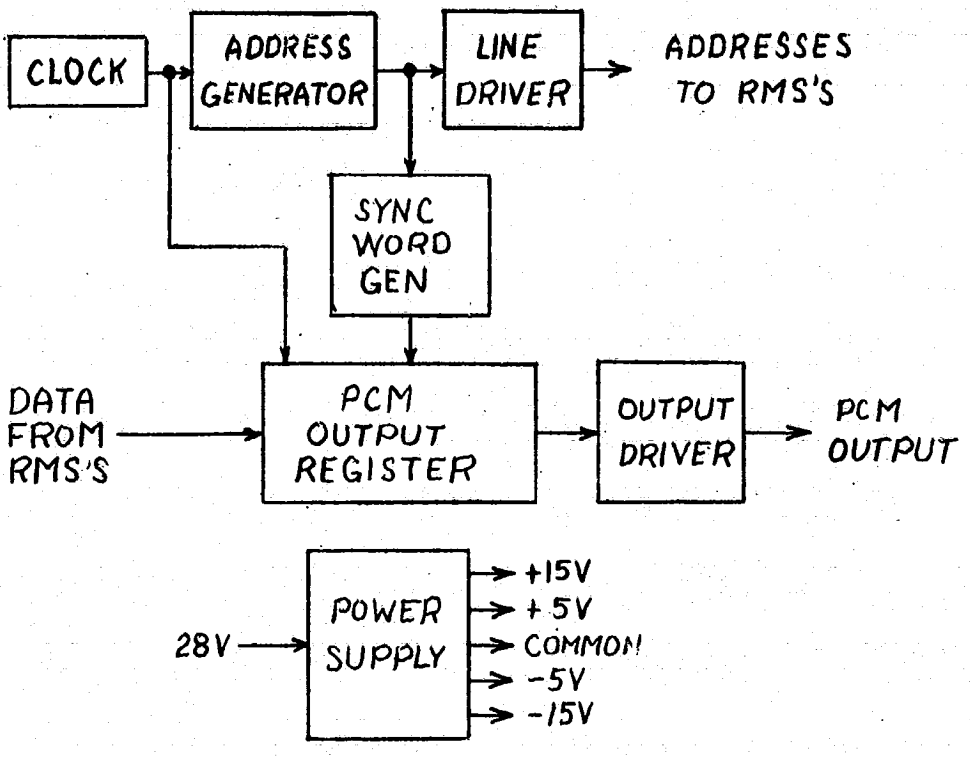


FIGURE V-2

BLOCK DIAGRAM

CENTRAL CONTROL UNIT

This format is similar to those presently in use.

The other blocks in the CCU are self explanatory.

Each remote measuring source (RMS) (Figure V-3) for configuration I consists of 4 eight-channel analog switch modules, 32 diode modules, an address processor, an amplifier, an analog-to-digital converter and line driver, and a power supply.

The CCU for configuration II is similar to that for configuration I except that redundant address line drivers and data input circuits are utilized.

The RMS for configuration II is similar to that for configuration I except that redundant address processor input circuits and redundant data output circuits are utilized.

The CCU for configuration III has an address generator that operates at twice the previous clock rate, but is "on-line" only half the time; redundant address line drivers with disconnect switching are use; the PCM data input circuit has redundant processors and a temporary data storage register; and the PCM output register has been modified to accept parallel data from the storage register.

The RMS for configuration III has an address processor similar to that used in configuration II but with slightly different connecctions to accommodate interleaved addresses and data. The A/D converter has extensive changes incorporated to accomplish interleaving of the addresses and data.

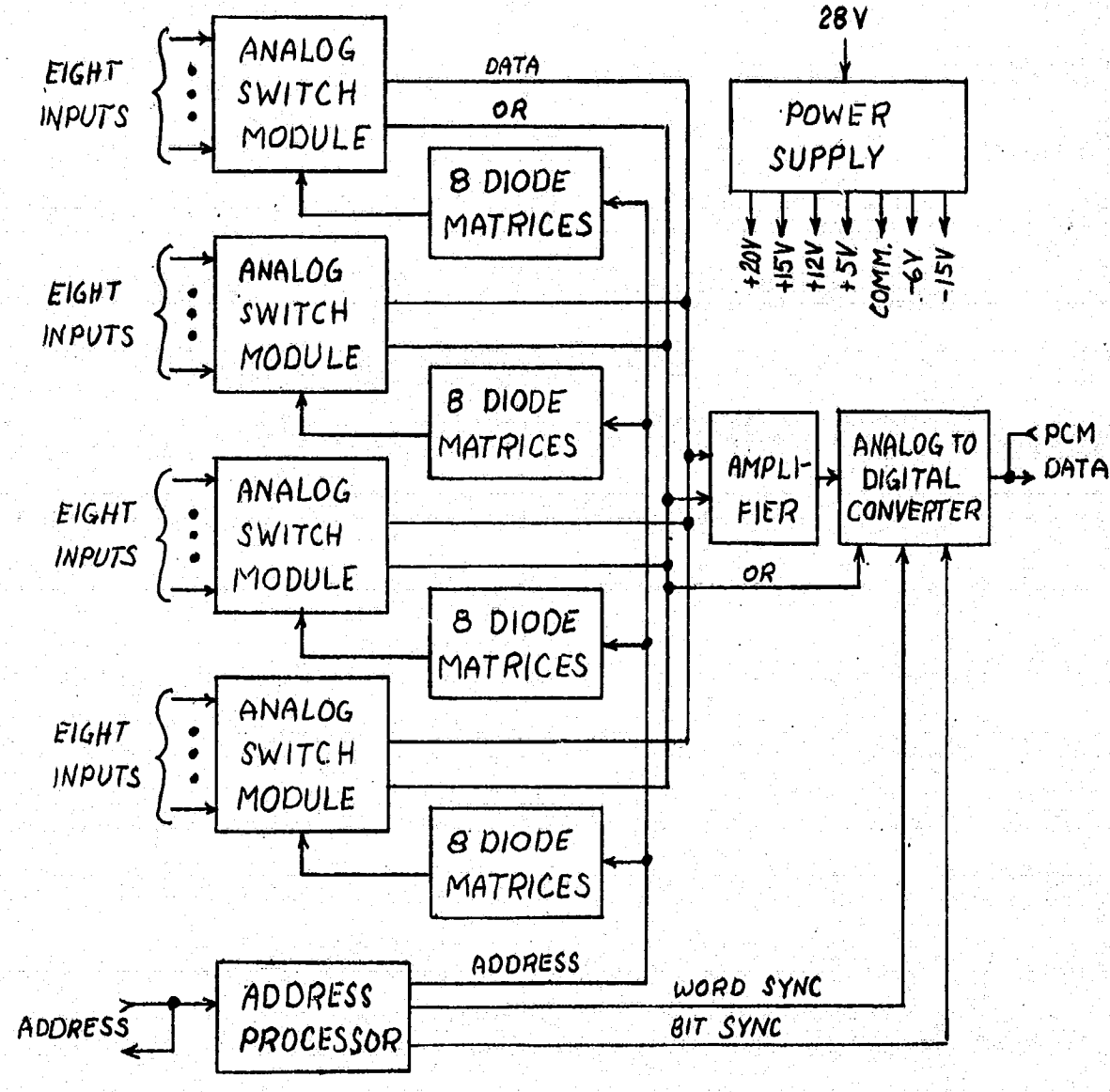


FIGURE V-3

BLOCK DIAGRAM

REMOTE MEASURING SOURCE I

Comparative Reliability for the Various Configurations

Table V-4 gives calculated failure rates for the configurations and cases analyzed. Examination of these failure rates produces the following information:

a. In all cases, configuration II has the lowest failure rate with III next and I last. Configuration III has less cabling but the additional synchronization circuitry raises its failure rate over that of configuration II.

b. When loss of any data is considered a system failure, case I, there is no significant difference in the configuration failure rates. However, in case 4, where loss of all data from all RMS's is considered a failure, configuration II is significantly superior to the other configurations and configuration III is superior to configuration I.

c. In case 4 where a failure is the loss of all data most of the failure rate is attributable to the central control unit.

TABLE V-4

DETAILED COMPARATIVE FAILURE RATES

Config. & Case	I-1	I-2	I-4	II-1	II-2	II-4	III-1	III-2	III-4
CCU									
Clock	.074	I-1	I-1	I-1	I-1	I-1	I-1	I-1	I-1
Address Gen.	.901	I-1	I-1	I-1	I-1	I-1	.944	III-1	III-1
Line Driver	.098	I-1	I-1	Red.	II-1	II-1	Red.	III-1	III-1
Sunc Wrd. Gen.	.597	I-1	I-1	I-1	I-1	I-1	.555	III-1	III-1
PCM Out, Reg. & Out. Dr.	.211	I-1	I-1	.205	II-1	II-1	.181	III-1	III-1
P.S.	.821	I-1	I-1	I-1	I-1	I-1	I-1	I-1	I-1
Data Input	-	-	-	-	-	-	.283	III-1	III-1
CCU TOTAL	2.74	I-1	I-1	2.63	II-1	II-1	2.89	III-1	III-1
RMS									
Sw. Mod.*	.634	.263	.043	I-1	I-2	I-4	I-1	I-2	I-4
Diode Mat. **	.005	.002	.0003	I-1	I-2	I-4	I-1	I-2	I-4
Addr. Proc.	.771	I-1	-	.652	II-1	-	.652	III-1	-
Amplifier	.410	I-1	-	I-1	I-1	-	I-1	I-1	-
A/D Conv.	1.274	I-1	.041	1.203	II-1	-	1.136	III-1	.02
P.S.	1.296	I-1	-	I-1	I-1	-	I-1	I-1	-
Clock	-	-	-	-	-	-	.074	III-1	-
RMS TOTAL	6.596	4.916	.260	6.405	4.724	.182	6.412	4.732	.2021
SYSTEM TOTAL	31.39	22.57	3.95	30.35	21.53	3.36	30.64	21.82	3.70

NOTES: These numbers have been rounded off. More precise numbers were used for the calculations in the appendix.

* There are four switch modules per RMS.

** There are thirty-two diode matrices per RMS.

VI. RECOMMENDATIONS FOR RELIABLE ADDRESSABLE DATA SYSTEMS

The recommended system configuration and circuitry depends on the system data rate, and how vital it is to obtain the data.

The analyses in Chapter V indicate that there is not much difference between the four configurations and that, for the configurations analyzed, the cable and connectors have a relatively minor effect on system reliability.

Therefore, for a system where the data is relatively unimportant, a configuration similar to configuration I would be recommended. It is the least complex and the lightest in weight.

When the data is of medium importance a configuration similar to that of Figure VI-1 is recommended. This is a parallel redundant system and while it is twice the weight of a single system, erroneous data from either output can generally be identified and the total failure rate then becomes the product of failure rates of each half. Thus, if configuration I is used for both halves, the failure rate for loss of any data becomes $\left[(31.388)(10)^{-6}\right]^2$ or 0.001 failures per million hours.

If the data is of vital importance, a triple redundant system can be used and the failure rate becomes $\left[(31.388)(10)^{-6}\right]^3$ or 0.000,000,03 failures per million hours.

In this data system where digital signals are transmitted between units via interconnecting cables, the interface circuitry

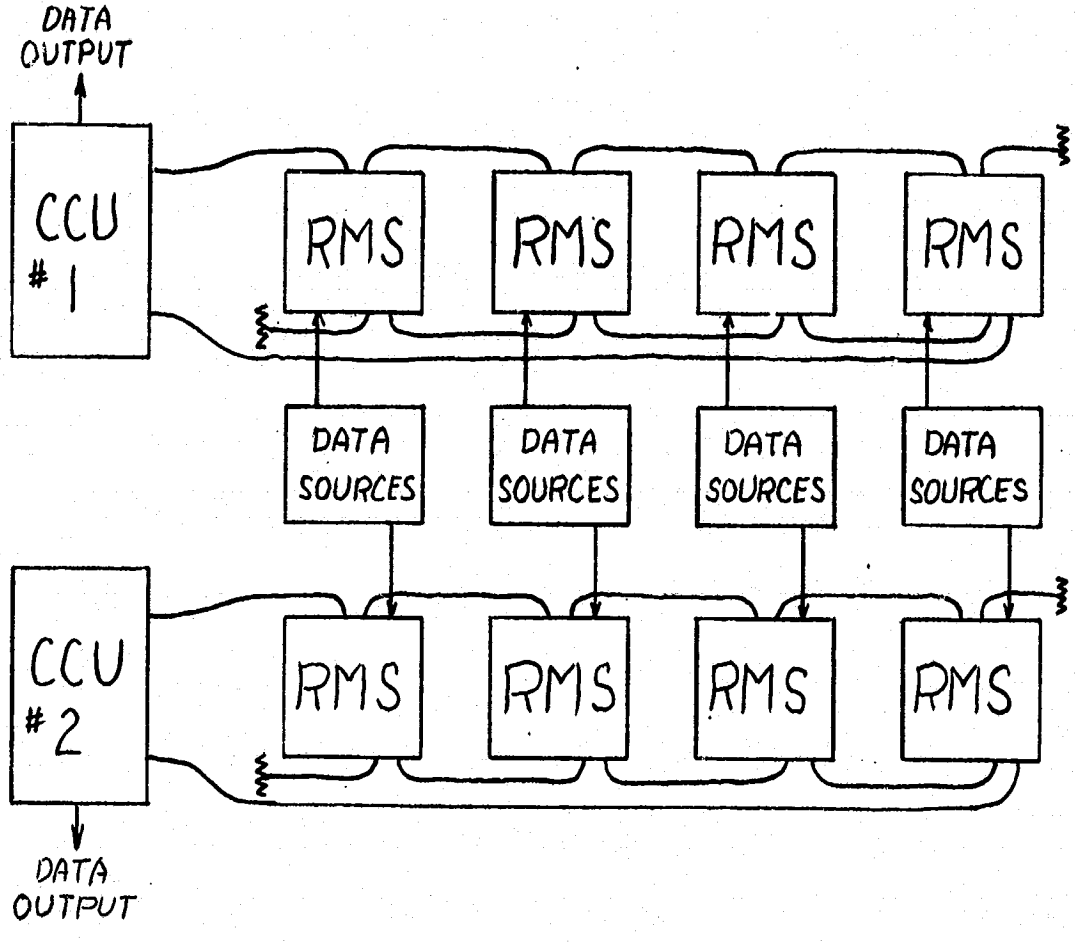


Figure VI-1, Parallel Redundant Configuration

used is affected to a considerable extent by the system data rate. Simpler circuits can be used in a low data rate system than in high data rate system. A high data rate system is one where twice the propagation delay over the longest path is more than one third of the shortest transmitted pulse width. This occurs at data rates of about 500 kilobits per second when the longest path is about 100 feet.

A high data rate system requires additional circuitry to detect broken cables. This is necessary to avoid improper operation caused by reflections from the fault. The usual result is generation of extra clock pulses in the RMS's. The circuitry for low data rate systems was used in the reliability analyses of Chapter V, but the relative merit of the configurations would remain about the same with the additional circuitry.

APPENDIX A

RELIABILITY CALCULATIONS

All failure rates in this appendix are per million hours.

CONFIGURATION I - Case 1

Description	N	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
CCU I-1	1	2.73914	-	1	2.73914
RMS I-1	4	6.59648	-	1	26.38592
Wire	276	.008	-	1	2.208
Connection, Sensor	256	.0001	-	1.8	.04608
Resistor, Terminating	2	.003	30	1.5	.009
					31.38814

CCU I - Case 1

Description	N	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
Clock	1	.07362	-	1	.07362
Address Generator I-1	1	.9013	-	1	.9013
Line Driver I-1	1	.09814	-	1	.09814
Sync Word Generator I-1	1	.5975	-	1	.5975
PCM Output Register I & Output Driver	1	.21086	-	1	.21086
Power Supply, CCU	1	.8211	-	1	.8211
P.C. Board	1	.01	-	1	.01
Connector, 2 pin	4	.0002	-	1.4	.00112
Case	1	.0005	-	1	.0005
Cover	1	.015	-	1	.015
Gasket	1	.01	-	1	.01
					2.73914

Description	N	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
Clock					
Transistor	2	.01	10	.07	.0014
Resistor, Metal Film	6	.003	10	.94	.01692
Capacitor, Porcelain	5	.004	20	.6	.012
Coil	1	.01	85°	2	.02
Crystal	1	.01	-	1	.01
Joint, Soldered	33	.0001	-	1	.0033
P.C. Board	1	.01	-	1	.01
					.07362
Address Generator I - Case 1					
I.C. Digital	42	.02	-	1	.84
Joint Soldered	513	.0001	-	1	.0513
P.C. Board	1	.01	-	1	.01
					.9013
Line Driver I-1					
Integrated Circuit	2	.02	-	1	.04
Transistor, Signal	4	.01	10	.1	.004
Transistor, Driver	2	.01	25	.07	.0014
Diode, Signal	2	.006	10	.1	.0012
Resistor, Metal Film	12	.003	10	.94	.03384
Joint, Soldered	77	.0001	-	1	.0077
P.C. Board	1	.01	-	1	.01
					.09814
Sync Word Generator I-1					
I.C. - Digital	28	.02	-	1	.56
Joint, Soldered	275	.0001	-	1	.0275
P.C. Board	1	.01	-	1	.01
					.5975
PCM Output Register I and Output Driver					
I.C. Digital	9	.02	-	1	.18
Transistor	1	.01	10	.07	.0007
Resistor, Metal Film	3	.003	10	.94	.00846
Joint, Soldered	117	.0001	-	1	.0117
P.C. Board	1	.01	-	1	.01
					.21086

(continued on next page)

Description	N	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
Power Supply - Central Unit					
Transformer, Power	1	.127	85°	.1	.0127
Inductor	3	.127	85°	.1	.0381
Transistor, Switching	7	.01	10	.07	.0049
Diode, Power	10	.006	50	.3	.018
Diode, Signal	2	.006	10	.1	.0012
Diode, Zener	1	.006	25	.2	.0012
Capacitor, Tantalum	9	.02	60	3.8	.684
Capacitor, Ceramic	1	.004	50	2.7	.0108
Resistor, Metal Film	11	.003	30	1.5	.0495
Joints, Soldered	7	.0001	-	1	.0007
					.8211

REMOTE MEASURING SOURCE I - Case 1

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
Switch Module I-1	4	.63444	1	2.53776
Diode Matrix I-1	32	.00488	1	.15616
Address Processor I-1	1	.77062	1	.77062
Amplifier	1	.40982	1	.40982
A to D Converter I-1	1	1.27412	1	1.27412
Power Supply, RMS	1	1.2959	1	1.2959
PC Board	1	.01	1	.01
Connector, 36 pin	2	.0036	16	.1152
Connector, 2 pin	5	.0002	1.4	.0014
Case	1	.0005	1	.0005
Cover	1	.015	1	.015
Gasket	1	.01	1	.01
				6.59648

Description	N	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
Switch Module I - Case 1					
I.C. Logic	2	.02	-	1	.04
Transistor, NPN	16	.01	10	.07	.0112
Transistor, PNP	8	.01	10	.07	.0056
Transistor, Dual MOSFET	16	.04	10	.07	.0448
Resistor, Metal Film	112	.003	10	.94	.31584
Capacitor, Porc. or Cer.	16	.004	20	.6	.0384
Capacitor, Tantalum, Solid	2	.02	60	3.8	.152
Diode, Signal	8	.006	10	.1	.0048
P.C. Board	1	.01	-	1	.01
Joint, Soldered	118	.0001	-	1	.0118
					.63444
Diode Matrix I - Case 1					
Diode	5	.006	10	.1	.003
Connector, 6 pin	1	.0006	-	2.3	.00138
Joint, Soldered	5	.0001	-	1	.0005
					.00488
Address Processor I - Case 1					
I.C., Linear	2	.02	-	1	.04
I.C., Digital	22	.02	-	1	.44
Transistor, NPN	2	.01	10	.07	.0014
Diode, Signal	4	.006	10	.1	.0024
Resistor, Metal Film	26	.003	10	.94	.07332
Capacitor, Cer. or Porc.	5	.004	20	.6	.012
Capacitor, Tantalum, Solid	2	.02	60	3.8	.152
P.C. Board	1	.01	-	1	.01
Joints, Soldered	395	.0001	-	1	.0395
					.77062
Amplifier					
Transistor, Dual FET	1	.04	10	.07	.0028
Transistor, Dual NPN	1	.02	10	.07	.0014
Transistor, Dual PNP	1	.02	10	.07	.0014
Transistor, MOSFET	1	.02	10	.07	.0014
Transistor, PNP	1	.01	10	.07	.0014
Transistor, NPN	1	.01	10	.07	.0007
Integrated Circuit Ampl.	1	.02	-	1	.02
I.C., Single Shot Multi.	1	.02	-	1	.02
Capacitor, Tant., Solid	2	.02	20	2.9	.116
	2	.02	60	3.8	.152
Capacitor, Cer. or Porc.	6	.004	20	.6	.0144
Resistor, Metal Film	21	.003	10	.94	.05922

(Continued on next page)

Description	N	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
Amplifier (Continued)					
Diode, Zener	1	.006	25	.2	.0012
Potentiometer	1	.004	10	1.8	.0072
Joint Soldered	7	.0001	-	1	.0007
P.C. Board	1	.01	-	1	.01
					.40982
Analog to Digital Converter					
I - Case 1					
Transistor	3	.02	10	.07	.0042
I.C., Linear	5	.02	-	1	.1
I.C., Digital	24	.02	-	1	.48
Driver, MOSFET	17	.02	-	1	.34
Transistor, Dual MOSFET	8	.04	10	.07	.0224
Diode, Signal	1	.006	10	.1	.0006
Diode, Zener	2	.006	50	.3	.0036
Capacitor, Cer. or Porc.	7	.004	20	.6	.0168
Capacitor, Tantalum, Solid	2	.02	60	3.8	.152
Resistor, Metal Film	31	.003	10	.94	.08742
Joints, Soldered	571	.0001	-	1	.0571
P.C. Board	1	.01	-	1	.01
					1.27412
Power Supply, RMS					
Transformer, Power	1	.127	85°	.1	.0127
Inductor	3	.127	85°	.1	.0381
Transistor, Linear	2	.01	25	.1	.002
Transistor, Switching	7	.01	10	.07	.0049
Diode, Power	8	.006	50	.3	.0144
Diode, Signal	7	.006	10	.1	.0042
Diode, Zener	3	.006	25	.2	.0036
I.C. Linear	2	.02	-	1	.04
Capacitor, Tantalum	13	.02	60	3.8	.988
Capacitor, Ceramic or Porc.	9	.004	50	2.7	.0972
Resistor, Metal Film	20	.003	30	1.5	.09
Joints, Soldered	8	.0001		1	.0008
					1.2959

CONFIGURATION I - Case 2 & 3

Description	N	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
CCU I-1	1	2.73914	-	1	2.73914
RMS I-2	4	4.9156	-	1	19.6624
Wire	20	.008	-	1	.16
Resistor, Terminating	2	.003	30	1.5	.009
					22.57054

REMOTE MEASURING SOURCE I - Case 2 & 3

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
Switch Module I-2	4	.26366	1	1.05464
Diode Matrix I-2	32	.0023		.0736
Address Processor I-1	1	.77062	1	.77062
Amplifier	1	.40982	1	.40982
A/D Converter I-1	1	1.27412	1	1.27412
Power Supply	1	1.2959	1	1.2959
P.C. Board	1	.01	1	.01
Connector, 36 pin	2	$.36(10)^{-6}$	16	$11.52(10)^{-6}$
Connector, 2 pin	5	.0002	1.4	.0014
Case, Cover & Gasket	1	.0255	1	.0255
				4.9156

Description	N	Mode	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
Switch Module - Case 2 & 3						
I.C. Logic	2	O	.013	-	1	.026
Transistor, NPN	16	S	.007	10	.07	.00784
Transistor, PNP	8	S	.007	10	.07	.00392
Transistor, Dual MOSFET	16	S	.026	10	.07	.02912
Resistor, Metal Film	112	S	.0003	10	.94	.03158
Capacitor, Porc. or Cer.	16	N	-	20	.6	-
Capacitor, Tantalum, Solid	2	E	.02	60	3.8	.152
Diode, Signal	8	S	.004	10	.1	.0032
P.C. Board	1	E	.01	-	1	.01
Joint, Soldered	118	N	-	-	1	-
						.26366

Description	N	Mode	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
Diode Matrix - Case 2 & 3						
Diode	5	S	.004	10	.1	.002
Connector, 6 pin	1	S	.0003	-	1	.0003
Joint, Soldered	5	-	-	-	1	-
						.0023

SYSTEM I - Case 4

Description	N	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
CCU I-1	1	2.73914	-	1	2.73914
RMS I-4	4	.25996	-	1	1.03984
Wire	20	.008	-	1	.16
Resistor, Terminating	2	.003	30	1.5	.009
					3.94798

REMOTE MEASURING SOURCE I - Case 4

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
Switch Module I-4	4	.04312	1	.17248
Diode Matrix I-4	32	.0003	1	.0096
Address Processor	1	-	1	-
Amplifier	1	-	1	-
A/D Converter I-4	1	.04098	1	.04098
Power Supply	1	-	1	-
P.C. Board	1	.01	1	.01
Connector, 36 pin	2	-	-	-
Connector, 2 pin	5	.0002	1.4	.0014
Case, Cover & Gasket	1	.0255	1	.0255
				.25996

Description	N	Mode	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
Switch Module I - Case 4						
I.C.	2	O	.013	-	1	.026
Transistor, NPN	8	S	.007	10	.07	.00392
Transistor, PNP	-					-
Transistor, Dual MOSFET	-					-
Resistor, M.F.	-					-
Capacitor, Porc. or Cer.	-					-
Capacitor, Tant., Solid	-					-
Diode, Signal	8	S	.004	10	.1	.0032
P.C. Board	1	E	.01		1	.01
Joint, Soldered	-					-
						.04312
Diode Matrix - Case 4						
Diode	-					-
Connector, 6 pin	1	S	.0003	-	1	.0003
						.0003
Address Module - Case 4	NO EFFECT					
Amplifier - Case 4	NO EFFECT					
A/D Converter I - Case 4						
Transistor	2	S	.007	10	.07	.00098
I.C.	2	E	.02	-	1	.04
						.04098
Power Supply - Case 4	NO EFFECT					

CONFIGURATION II - Case 1

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
CCU II-1	1	2.6347	1	2.6347
RMS II-1	4	6.40484	1	25.61936
Wire (sensors)	256	.008	1	2.048
Connection (sensors)	256	.0001	1.8	.04608
				30.34814

CCU II - Case 1

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
Clock	1	.07362	1	.07362
Address Generator I-1	1	.9013	1	.9013
Line Driver I (Parallel Redundant)	2	.09814	Prod.	$.0096(10)^{-6}$
Sync Word Generator I-1	1	.5975	1	.5975
PCM Output Register II & Output Driver	1	.20512	1	.20512
Power Supply	1	.8211	1	.8211
P.C. Board	1	.01	1	.01
Connector, 2 pin	2*	.0002	1.4	.00056
Case, Cover & Gasket	1	.0255	1	.0255
				2.6347

* Address Output & Data Input connectors are redundant

PCM OUTPUT REGISTER II & OUTPUT DRIVER - Case 1

Description	N	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
I.C. Digital	9	.02	-	1	.18
Transistor (Parallel)	2	.01	10	.07	-
Resistor, Metal Film (Not Redundant)	1	.003	10	.94	.00282
Joint, Soldered (Not Redundant)	123	.0001	-	1	.0123
P.C. Board	1	.01	-	1	.01
					.20512

RMS II - Case 1

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
Switch Module I-1	4	.63444	1	2.53776
Diode Matrix I-1	32	.00488	1	.15616
Address Processor II-1	1	.65162	1	.65162
Amplifier	1	.40982	1	.40982
A to D Converter II-1	1	1.2026	1	1.2026
Power Supply	1	1.2959	1	1.2959
P.C. Board	1	.01	1	.01
Connector, 36 pin	2	.0036	16	.1152
Connector, 2 pin	1**	.0002	1.4	.00028
Case	1	.0005	1	.0005
Cover	1	.015	1	.015
Gasket	1	.01	1	.01
				6.40484

** Address & Data Connectors are redundant

Description	N	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
Address Processor II - Case 1					
Parallel Redundant Input Circuits	2	.15334	-	Product	$.0235(10)^{-6}$
I.C.	22	.02	-	1	.44
Transistor	2	.01	10	.07	.0014
Resistor, M.F.	6	.003	10	.94	.01692
Capacitor, Tantalum	2	.02	60	3.8	.152
P.C. Board	1	.01	-	1	.01
Joint, Soldered	313	.0001	-	1	.0313
					.65162
Input Circuit					
I.C.	3	.02	-	1	.06
Diode, Signal	6	.006	10	.1	.0036
Capacitor, Cer. or Porc.	3	.004	20	.6	.0072
Resistor, Metal Film	22	.003	10	.94	.06204
Joint, Soldered	105	.0001	-	1	.0105
P.C. Board	1	.01	-	1	.01
					.15334

(Continued on next page)

Description	N	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
Analog to Digital Converter II - Case 1					
Transistor, FET	1	.02	10	.07	.0014
I.C., Analog	4	.02	-	1	.08
I.C., Digital	22	.02	-	1	.44
Driver, MOSFET	17	.02	-	1	.34
Transistor, Dual MOSFET	8	.04	10	.07	.0224
Output Circuit	2	.07148		Product	-
Diode, Signal	1	.006	10	.1	.0006
Diode, Zener	2	.006	50	.3	.0036
Capacitor, Cer. or Porc.	7	.004	20	.6	.0168
Capacitor, Tantalum, Solid	2	.02	60	3.8	.152
Resistor, Metal Film	30	.003	10	.94	.0846
P.C. Board	1	.01	-	1	.01
Joints, Soldered	512	.0001	-	1	.0512
					1.2026
Parallel Redundant Output Circuit					
Transistor, NPN or PNP	2	.02	10	.94	.0376
I.C., Digital	1	.02	-	1	.02
Resistor, Metal Film	4	.003	10	.94	.01128
Joint, Soldered	26	.0001	-	1	.0026
					.07148

CONFIGURATION II - Case 2 & 3

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
CCU II-1	1	2.6347	1	2.6347
RMS II-2	4	4.72397	1	18.89588
				21.53058

RMS II - Case 2

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
Switch Module I-2	4	.26366	1	1.05464
Diode Matrix I-2	32	.0023	1	.0736
Address Processor II-1	1	.65162	1	.65162
Amplifier	1	.40982	1	.40982
A/D Converter II-1	1	1.2026	1	1.2026
Power Supply	1	1.2959	1	1.2959
P.C. Board	1	.01	1	.01
Connector, 36 pin	2	$.36(10)^{-6}$	16	$11.52(10)^{-6}$
Connector, 2 pin	1	.0002	1.4	.00028
Case, Cover & Gasket	1	.0255	1	.0255
				4.72397

CONFIGURATION II - Case 4

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
CCU II-1	1	2.6347	1	2.6347
RMS II-4	4	.18208	1	.72832
				3.36302

REMOTE MEASURING SOURCE II - Case 4

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
Switch Module I-4	4	.04312	1	.17248
Diode Matrix I-4	32	.0003	1	.0096
Address Processor II-1	1	-		-
Amplifier	1	-		-
A/D Converter II-1	1	-		-
Power Supply	1	-		-
P.C. Board	1	-		-
Connector, 36 pin	2	-		-
Connector, 2 pin	1	-		-
Case, Cover, & Gasket	1	-		-
				.18208

CONFIGURATION III - Case 1

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
CCU III-1	1	2.89324	1	2.89324
RMS III-1	4	6.41228	1	25.64912
Wire (sensors)	256	.008	1	2.048
Connection (sensors)	256	.0001	1.8	.04608
				30.63644

CCU III - Case 1

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
Clock	1	.07362	1	.07362
Address Generator III-1	1	.9437	1	.9437
Line Driver III-1 (Redundant)	2	.18812	Prod.	-
Sync Word Generator III-1	1	.5551	1	.5551
PCM Output Register III-1 & Driver	1	.1809	1	.1809
Power Supply	1	.8211	1	.8211
P.C. Board	1	.01	1	.01
Connector, 2 pin	2*	.0002	1.4	.00056
Case, Cover & Gasket	1	.0255	1	.0255
Data Input Circuit III-1	1	.28276	1	.28276
				2.89324

* Address & Data Connectors are redundant

Description	N	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
Address Generator III - Case 1					
I.C. Digital	44	.02	-	1	.88
Joint Soldered	537	.0001	-	1	.0537
P.C. Board	1	.01	-	1	.01
					.9437
CCU Line Driver III - Case 1					
Integrated Circuit	3	.02	-	1	.06
Transistor, Switching	6	.01	10	.1	.06

(Continued on next page)

Description	N	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
CCU Line Driver III (Continued)					
Transistor, Driver	2	.01	25	.07	.0014
Diode, Signal	2	.006	10	.1	.0012
Resistor, Metal Film	16	.003	10	.94	.04512
P.C. Board	1	.01	-	1	.01
Joint, Soldered	104	.0001	-	1	.0104
					.18812
Sync Word Generator III - Case 1					
I.C.	26	.02	-	1	.52
Joint, Soldered	251	.0001	-	1	.0251
P.C. Board	1	.01	-	1	.01
PCM Output Register III and Output Driver - Case 1					
I.C.	8	.02	-	1	.16
P.C. Board	1	.01	-	1	.01
Joint, Soldered	109	.0001	-	1	.0109
					.1809
Data Input Circuit III - Case 1					
I.C.	10	.02	-	1	.2
Input Circuit	2	.08256	-	Prod.	$.006(10)^{-6}$
Joint, Soldered	146	.0001	-	1	.0146
P.C. Board	1	.01	-	1	.01
Resistor, Metal Film	2	.003	10	.94	.0564
Capacitor, Ceramic	2	.004	10	.22	.00176
					.28276
Input Circuit					
I.C.	3	.02	-	1	.06
Transistor	1	.01	10	.07	.0007
Resistor, Metal Film	5	.003	10	.94	.0141
Capacitor, Ceramic	2	.004	10	.22	.00176
Joint, Soldered	60	.0001	-	1	.006
					.08256

RMS III - Case 1

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
Switch Module I-1	4	.63444	1	2.53776
Diode Matrix I-1	32	.00488	1	.15616
Address Processor III-1 (same G_{FR} as II-1)	1	.65162	1	.65162
Amplifier	1	.40982	1	.40982
A to D Converter III-1	1	1.13642	1	1.13642
Power Supply	1	1.2959	1	1.2959
P.C. Board	1	.01	1	.01
Connector, 36 pin	2	.0036	16	.1152
Connector, 2 pin	1**	.0002	1.4	.00028
Case, Cover & Gasket	1	.0255	1	.0255
Clock Generator	1	.07362	1	.07362
				6.41228

** Address and data connectors are redundant

A/D CONVERTER III - Case 1

Description	N	G_{FR}	% Stress	K_A	$NG_{FR}K_A$
I.C.	38	.02	-	1	.76
MOSFET Driver	17	.02	10	.07	.0238
MOSFET, Dual	8	.04	10	.07	.0224
Capacitor, Ceramic	7	.004	20	.6	.0168
Capacitor, Tantalum	2	.02	60	3.8	.152
Resistor, Metal Film	31	.003	10	.94	.08742
Transistor	1	.01	10	.07	.0007
Diode	1	.006	10	.1	.0006
P.C. Board	1	.01	-	1	.01
Joint, Soldered	627	.0001	-	1	.0627
					1.13642

CONFIGURATION III - Case 2 & 3

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
CCU III-1	1	2.89324	1	2.89324
RMS III-2	4	4.7315	1	18.926
				21.81924

RMS III - Case 2

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
Switch Module I-2	4	.26366	1	1.05464
Diode Matrix I-2	32	.0023	1	.0736
Address Processor III-1	1	.65162	1	.65162
Amplifier	1	.40982	1	.40982
A/D Converter III-1	1	1.13642	1	1.13642
Power Supply	1	1.2959	1	1.2959
P.C. Board	1	.01	1	.01
Connector, 36 pin	2	$.36(10)^{-6}$	16	.00001
Connector, 2 pin	1	.0002	1.4	.00028
Case, Cover & Gasket	1	.0255	1	.0255
Clock	1	.07362	1	.07362
				4.7315

CONFIGURATION III - Case 4

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
CCU III-1	1	2.89324	1	2.89324
RMS III-4	4	.20208	1	.80832
				3.70156

REMOTE MEASURING SOURCE III - Case 4

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
Switch Module I-4	4	.0432	1	.17248
Diode Matrix I-4	32	..0003	1	.0096
Address Processor III-1	1	-		-
Amplifier	1	-		-
A/D Converter III-4	1	.02	1	.02
Power Supply	1	-		-
P.C. Board	1	-		-
Connector, 36 pin	2	-		-
Connector, 2 pin	1	-		-
Case, Cover & Gasket	1	-		-
Clock Generator	1	-		-
				.20208

A/D CONVERTER III - Case 4

Description	N	G_{FR}	K_A	$NG_{FR}K_A$
I.C.	1	.02	1	.02

APPENDIX B

CONFIGURATION DESCRIPTIONS

Configuration I -- The block diagrams are shown in Figure B-1. The only difference between A and B is the interconnection for equal delays in B. The block diagram of the central control unit is shown in Figure B-2. Figures B-3 through B-8 are the block or circuit diagrams of the various circuits in the CCU. Figure B-9 is the block diagram of the RMS and Figures B-10 through B-15 are the block and circuit diagrams for the RMS.

Configuration II -- Figure B-16 shows the block diagram for the configuration. Figure B-17 is the block diagram of the CCU for this configuration. All circuits for the CCU are the same as for configuration I, except the output register, Figure B-18, which has two data input circuits. The two line drivers are the same as the one used in configuration I. Figure B-19 shows the block diagram for an RMS. It uses the same circuits as configuration I, except for the address processor, Figure B-20, and the A/D converter, Figure B-21. These circuits are the same as for configuration I, except for the two input circuits for the address processor and two output circuits for the A/D converter.

Configuration III -- Figure B-22 shows the block diagram for configuration III. The CCU block diagram, Figure B-23, has a number of different circuits from the other CCUs. These changes are required to use the same line for both addresses and data. The address generator, Figure B-24, is similar to the other configurations, except for the addition of the address enable circuits for interleaved addresses and data. The address line driver, Figure B-25,

has two additional circuits to turn off the output, except when addresses are being transmitted. The input circuit, Figure B-26, is new and contains a data storage register to allow the data input from the RMSs to be at a faster clock rate than the PCM output from the CCU. It also contains the circuitry to recover the data and its clock rate from the Manchester coded data received from the RMSs. The output register, Figure B-27, is the same as before, but without the data input circuitry. Figure B-28 shows the block diagram for the configuration III RMS. It differs from the other RMSs in the address processor and A/D converter. The address processor, Figure B-29, is the same as that used in configuration II, except address transfer is obtained from the A/D converter. The A/D converter block diagram is shown in Figure B-30. It contains the control circuitry for receiving addresses and for transmitting data on the same cable. These circuits are shown in more detail in Figures B-31, B-32, B-33, and B-34. The counter shown in B-31 controls the successive approximation conversion, B-32 shows the convert register, B-32 shows the output gating, and B-34 shows the control circuitry. The operation of these circuits is initiated by receipt of an address sync pulse. It then counts using the trailing edge of the derived address clock; and on the tenth clock pulse, it provides an address transfer signal to the address processor. One half-bit later, it resets the decode enable and enables the A/D converter if the RMS has been addressed. After the A/D conversion and transmission of

the data, the control is reset and waits for the next address word sync signal. The A/D output circuit shown in Figure B-33 converts the NRZ data to Manchester code.

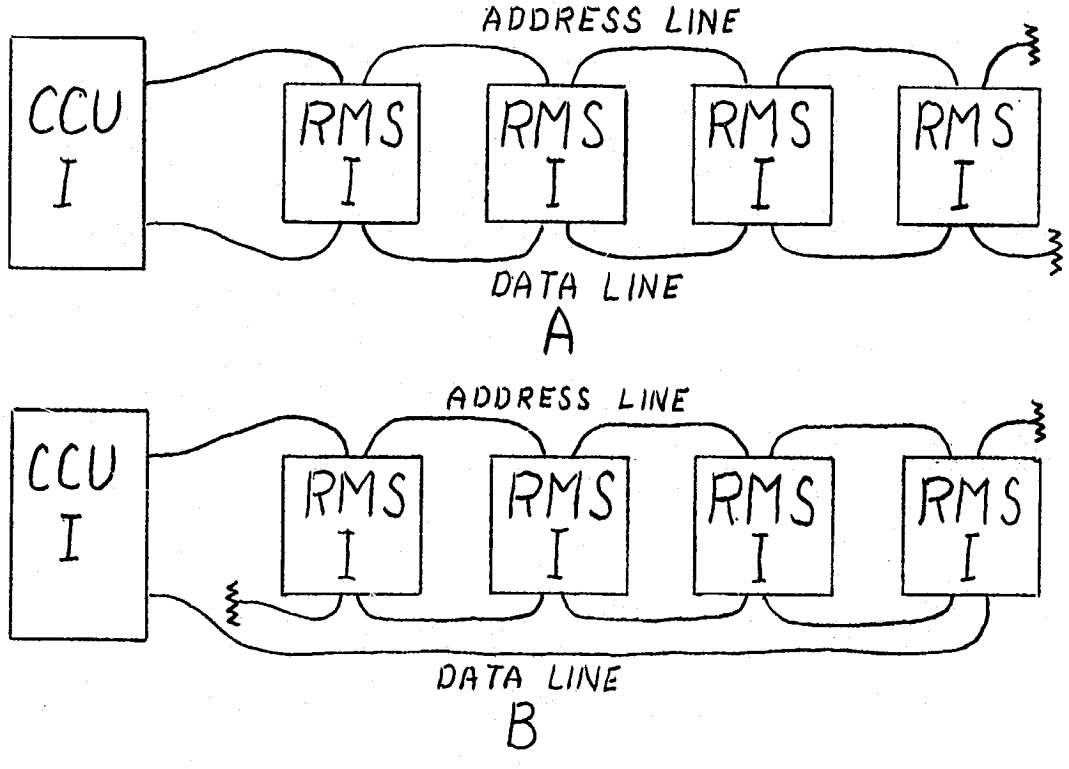


Figure B-1, Block Diagram Configuration I

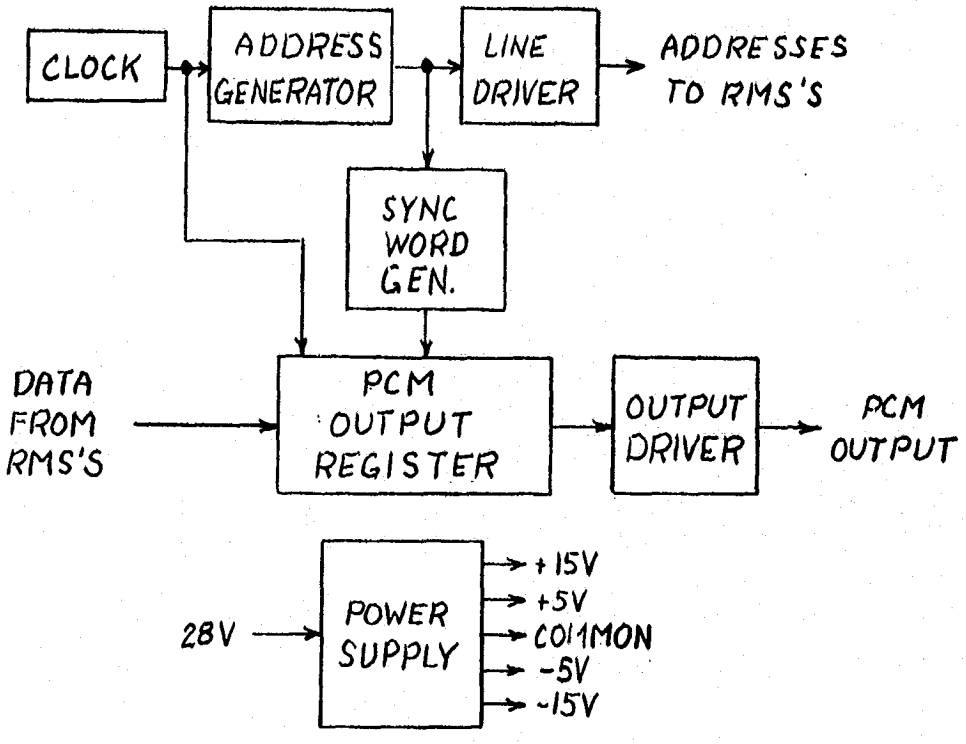


Figure B-2, Block Diagram, Central Control Unit I

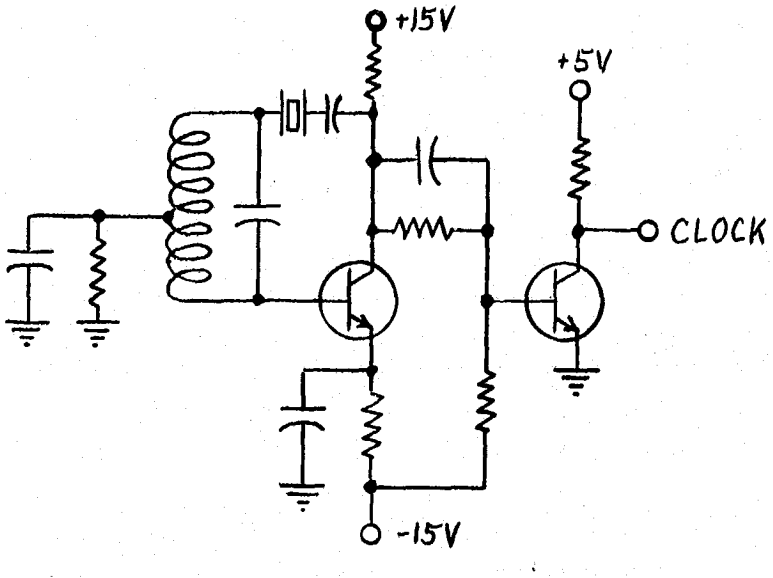


Figure B-3, Clock

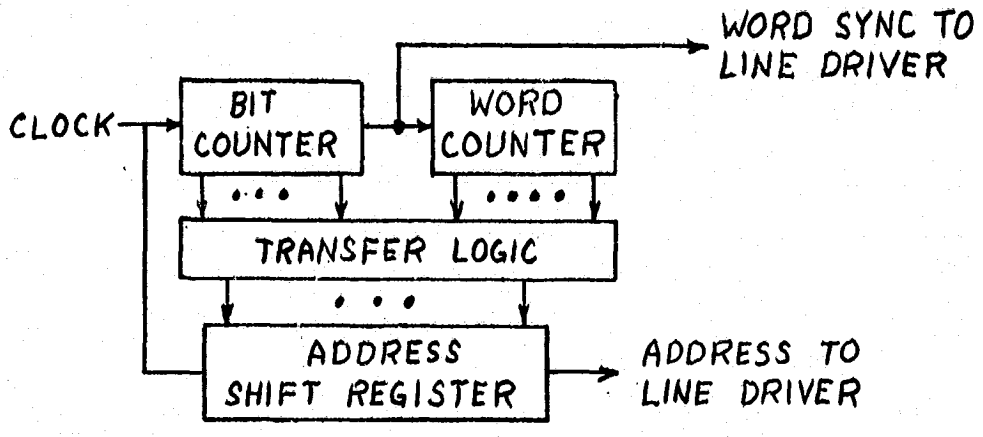


Figure B-4, Address Generator I

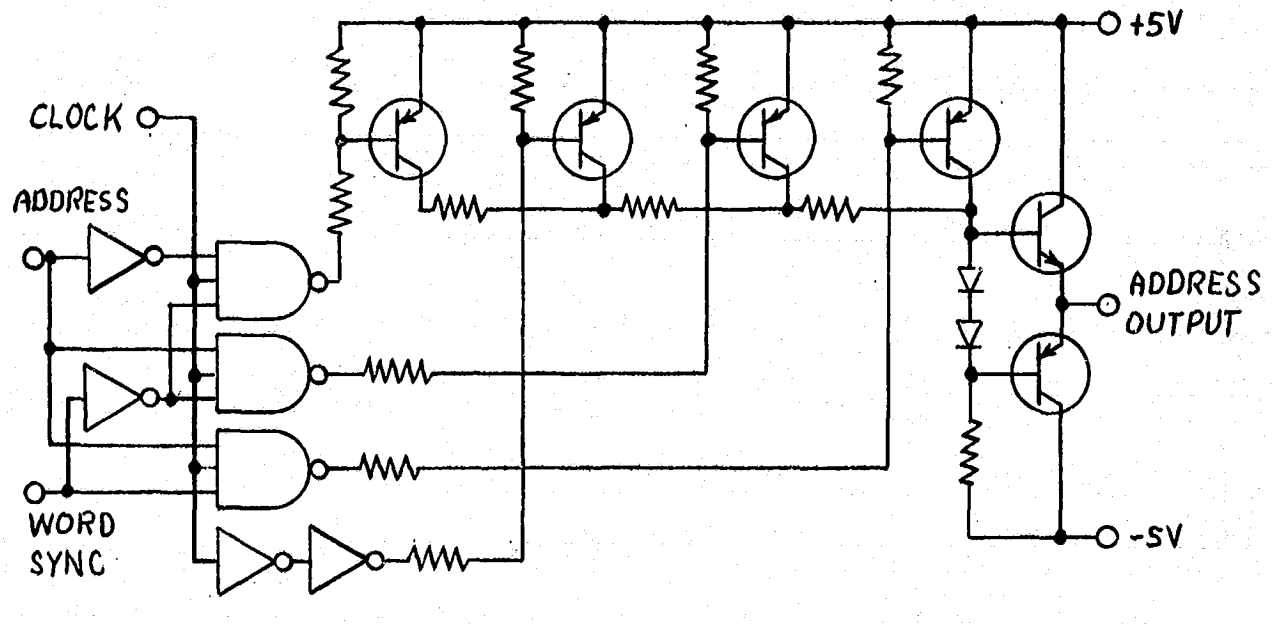


Figure B-5, Line Driver I

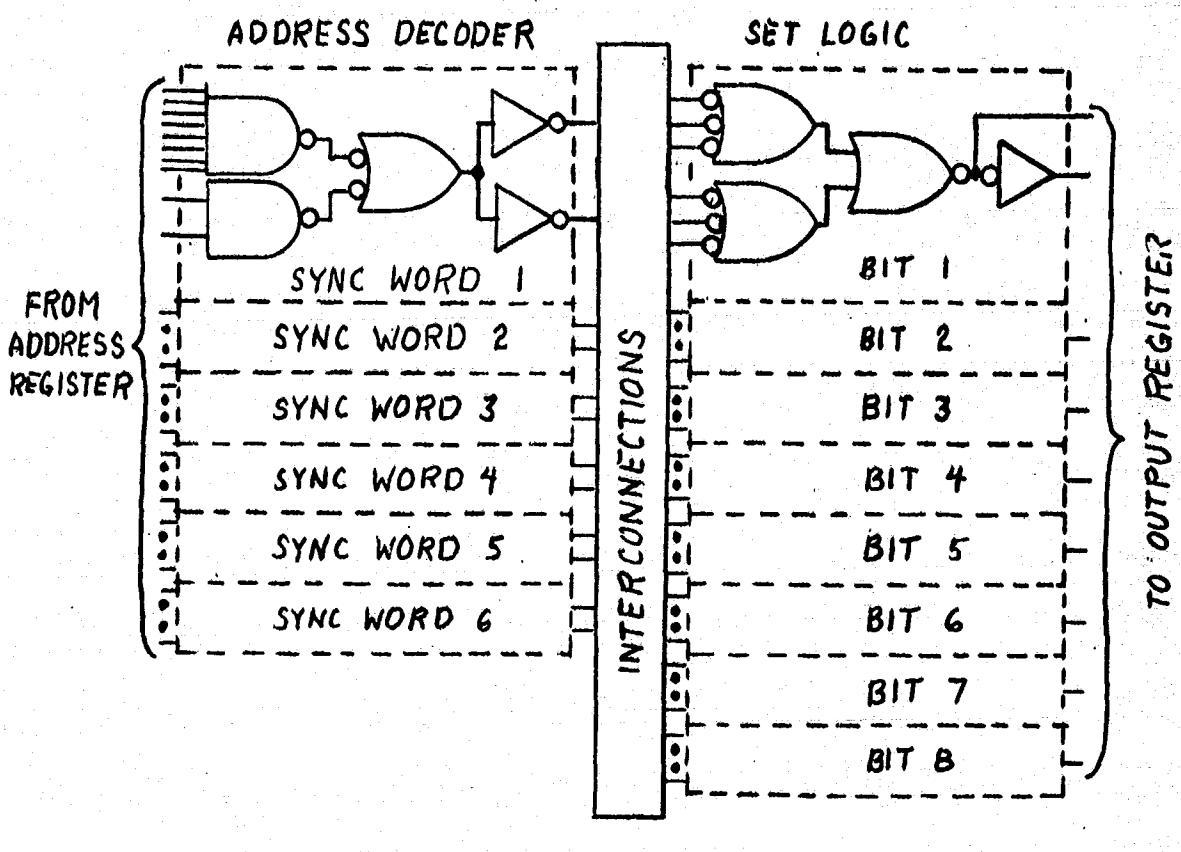


Figure B-6, Sync Word Generator I

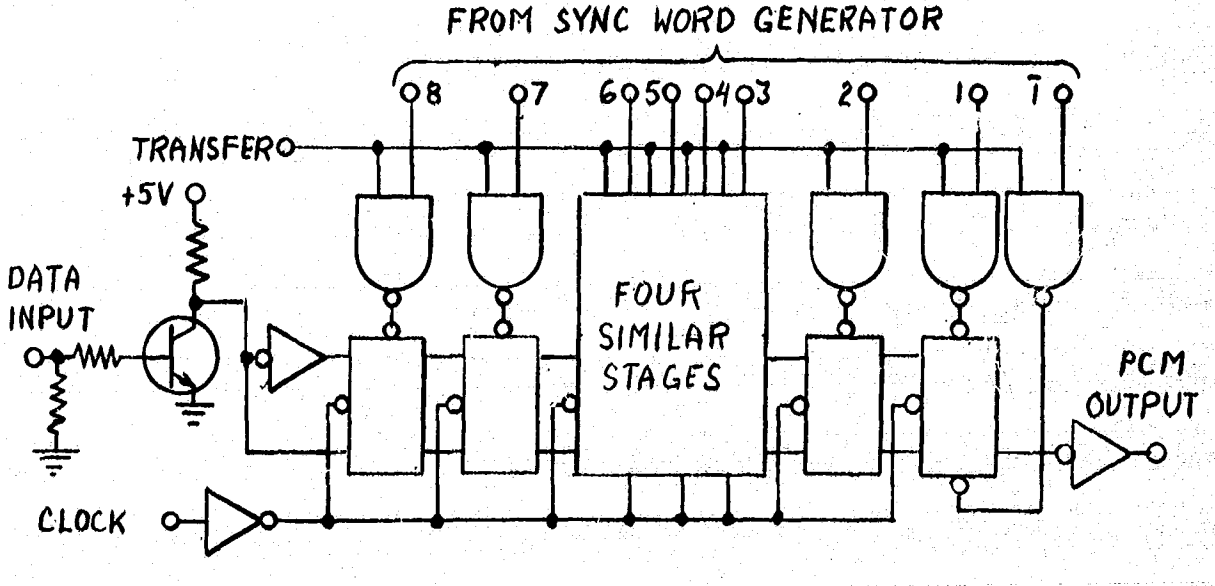


Figure B-7, PCM Output Register I & Output Driver

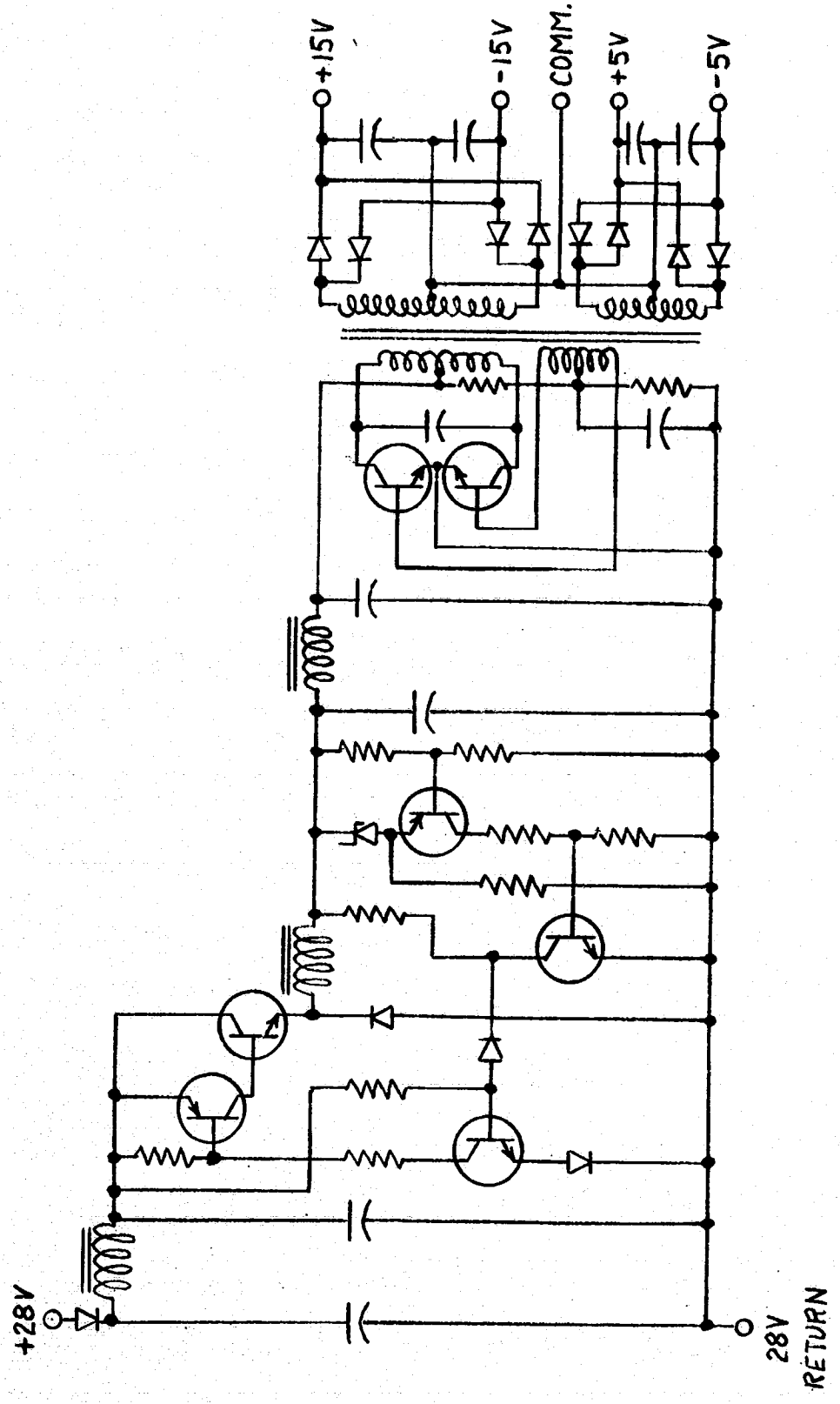


Figure B-8, CCU Power Supply

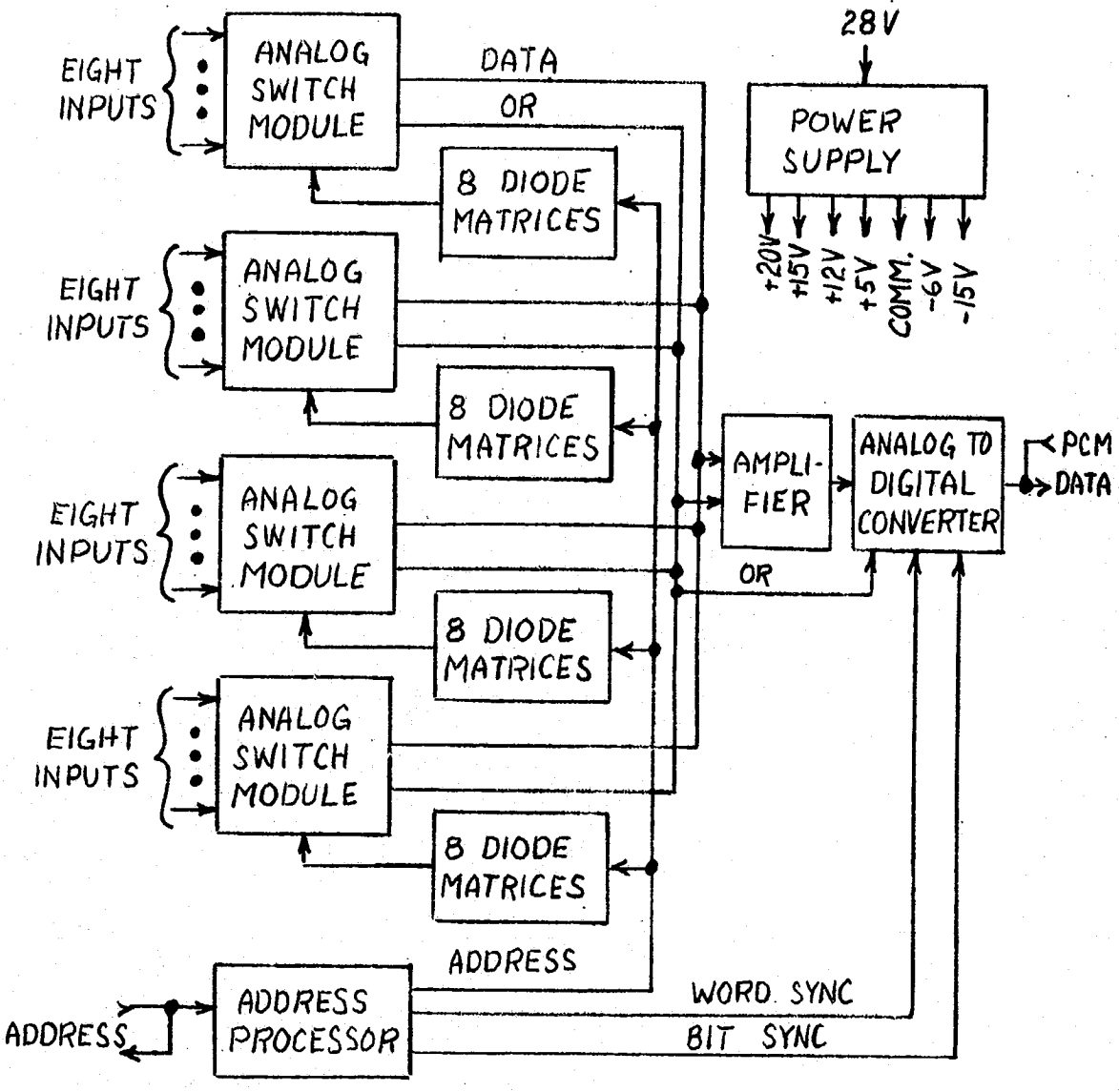


Figure B-9, Remote Measuring Source I

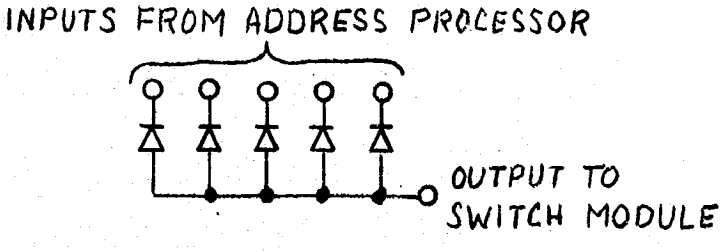


Figure B-10, Diode Matrix

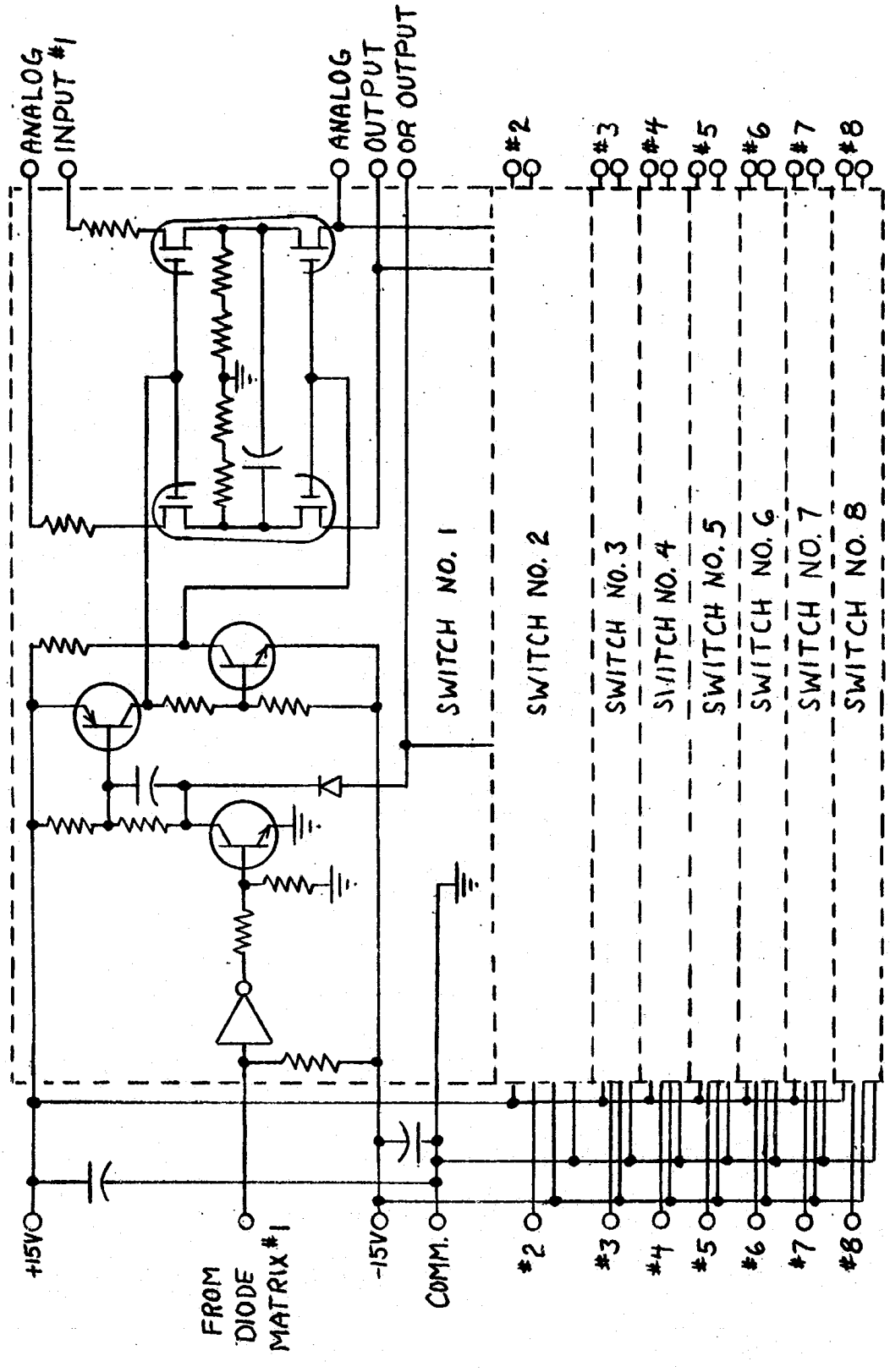


Figure B-11, Analog Switch Module

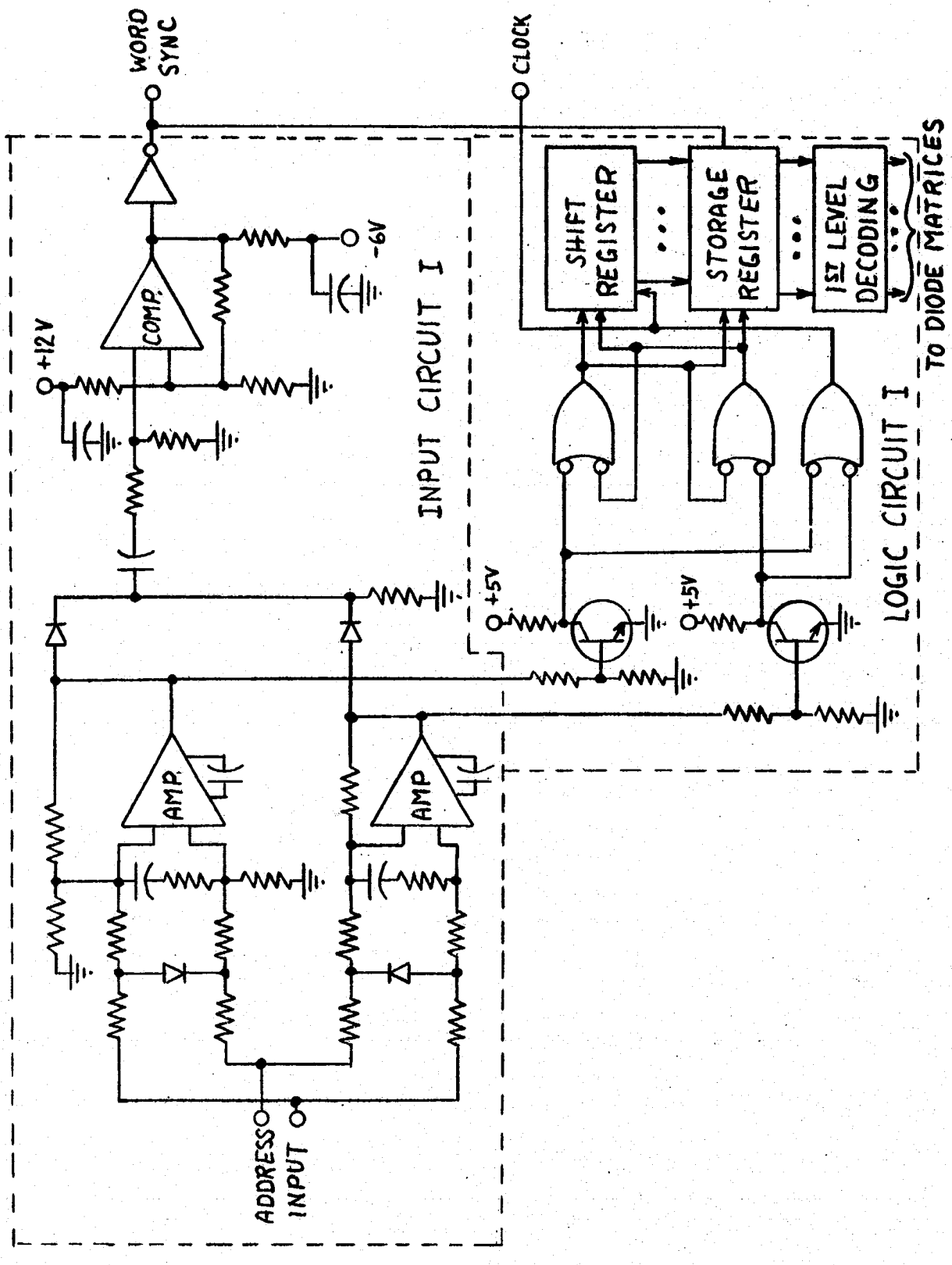


Figure B-12, Address Processor I

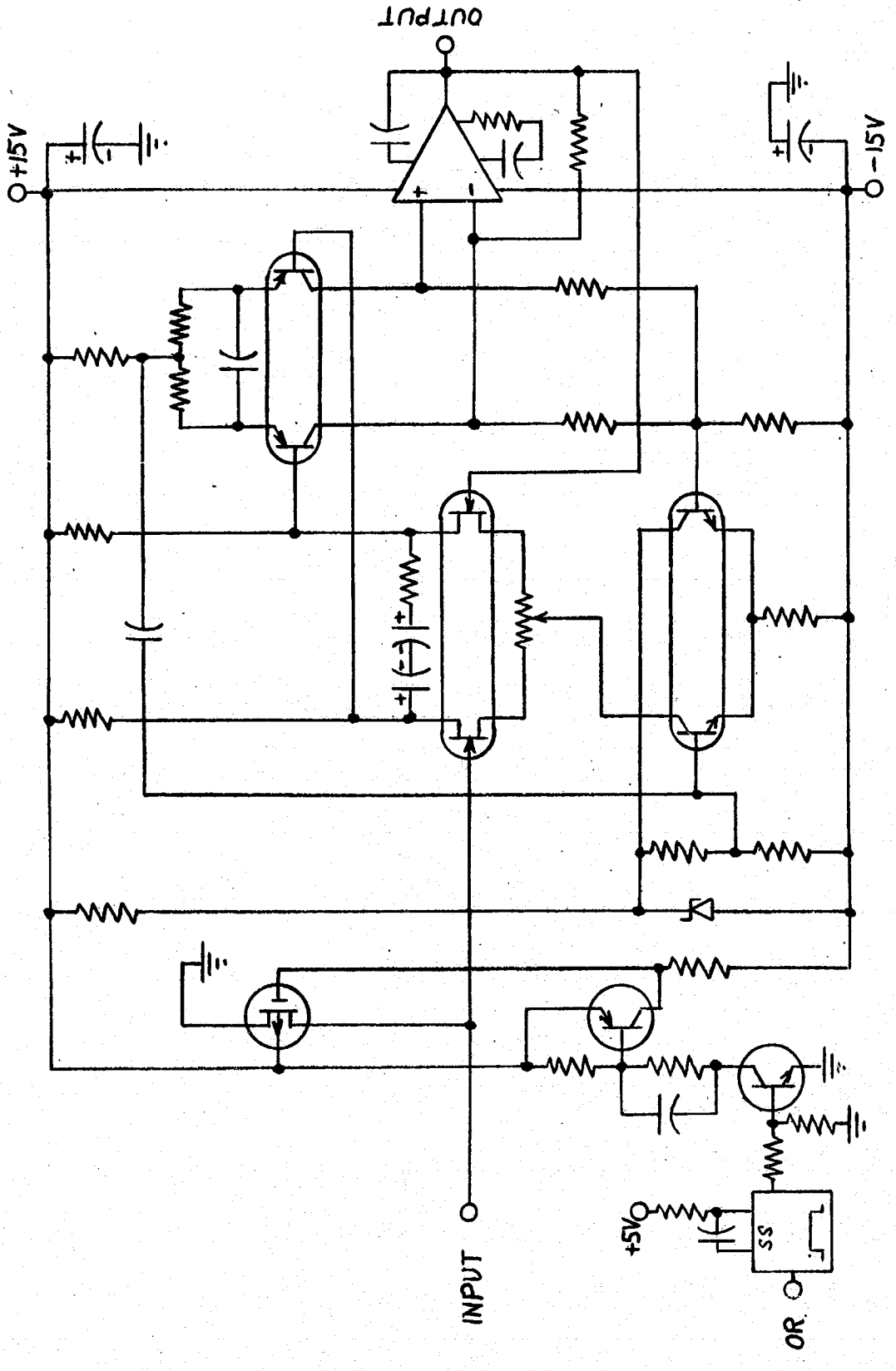


Figure B-13, Amplifier

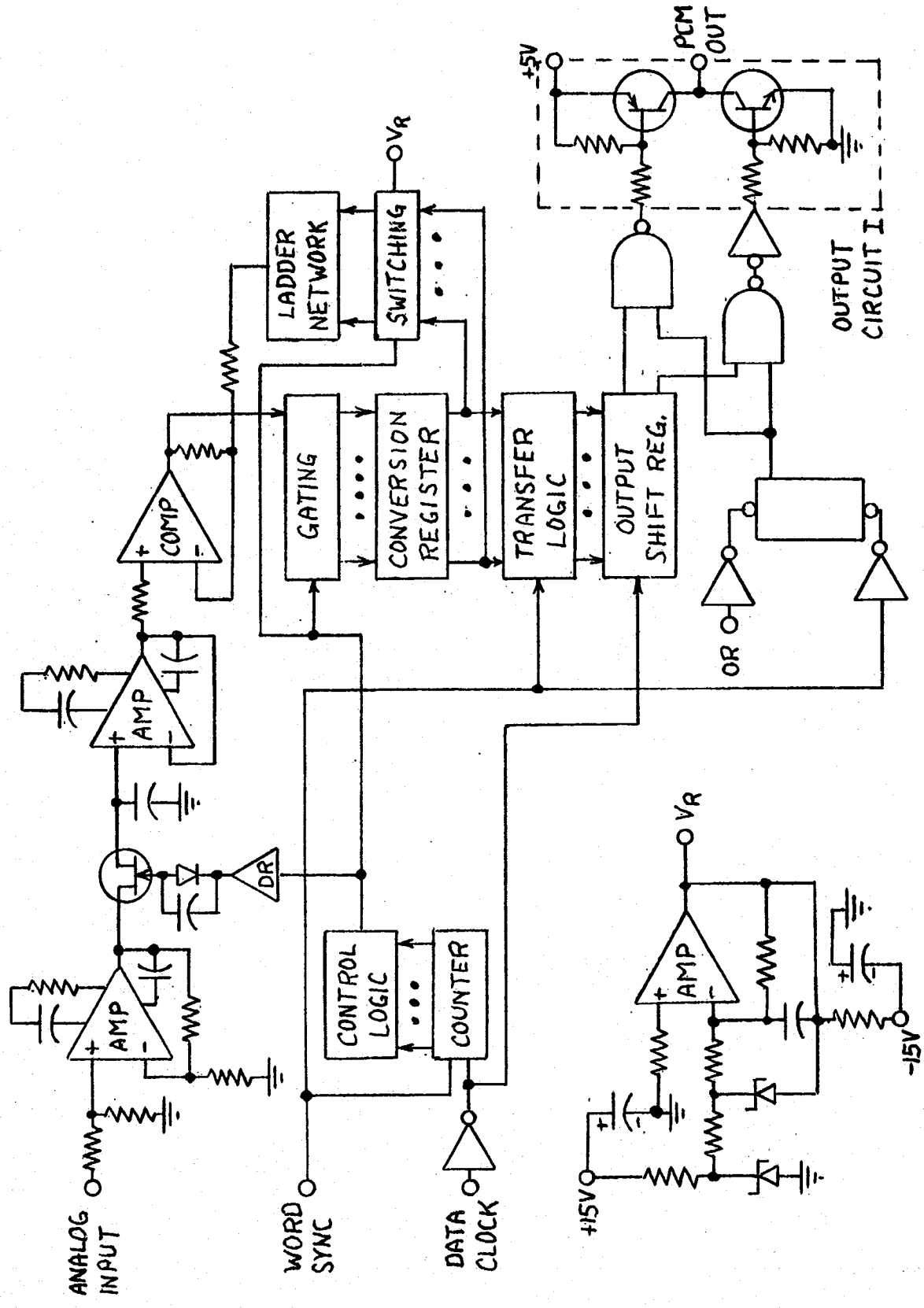


Figure B-14, Analog to Digital Converter I

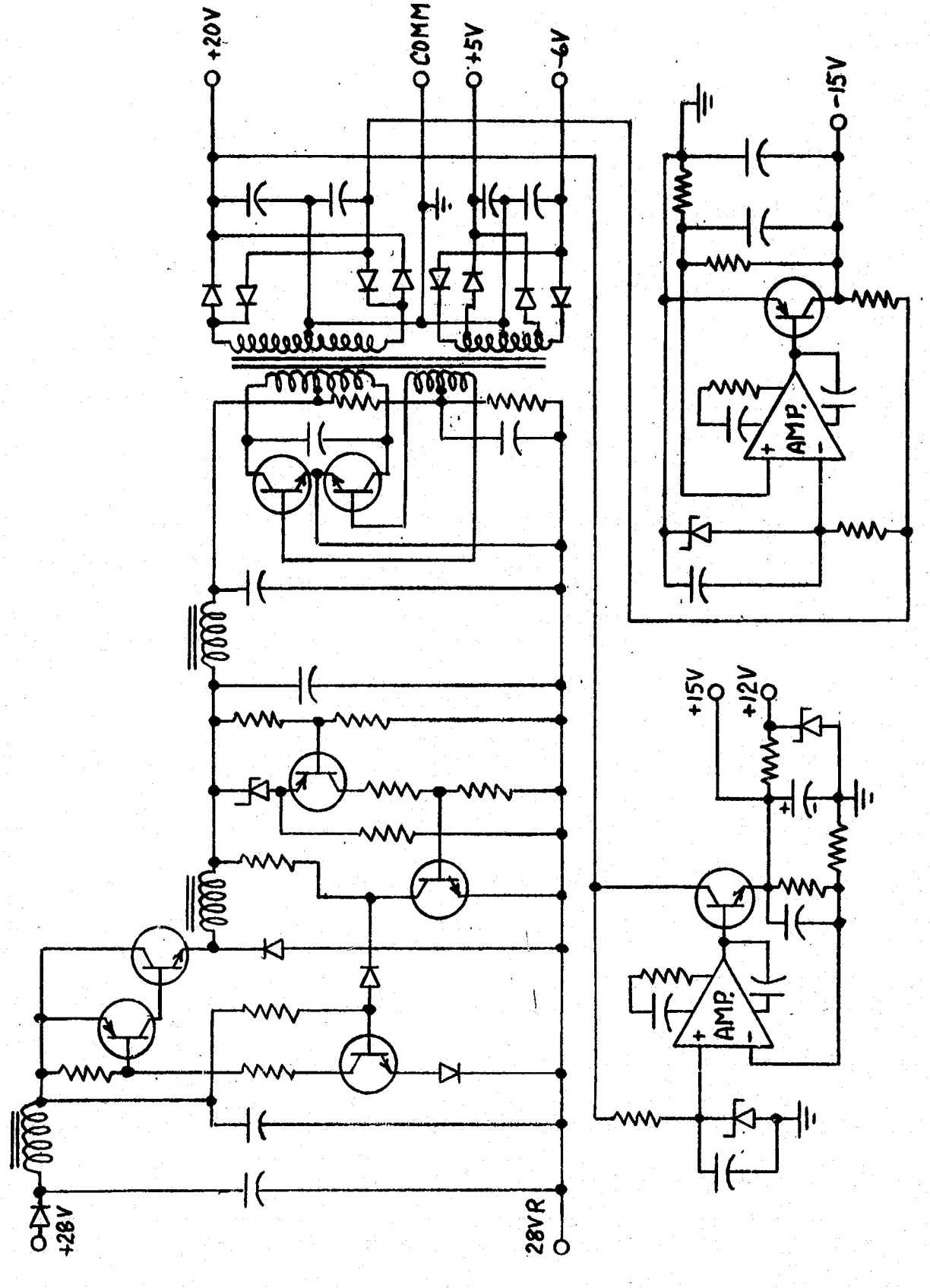


Figure B-15, RMS Power Supply

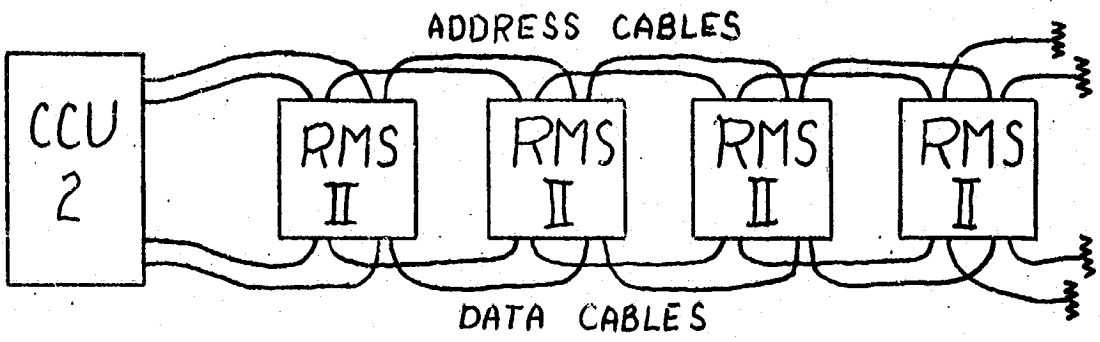


Figure B-16, Configuration II

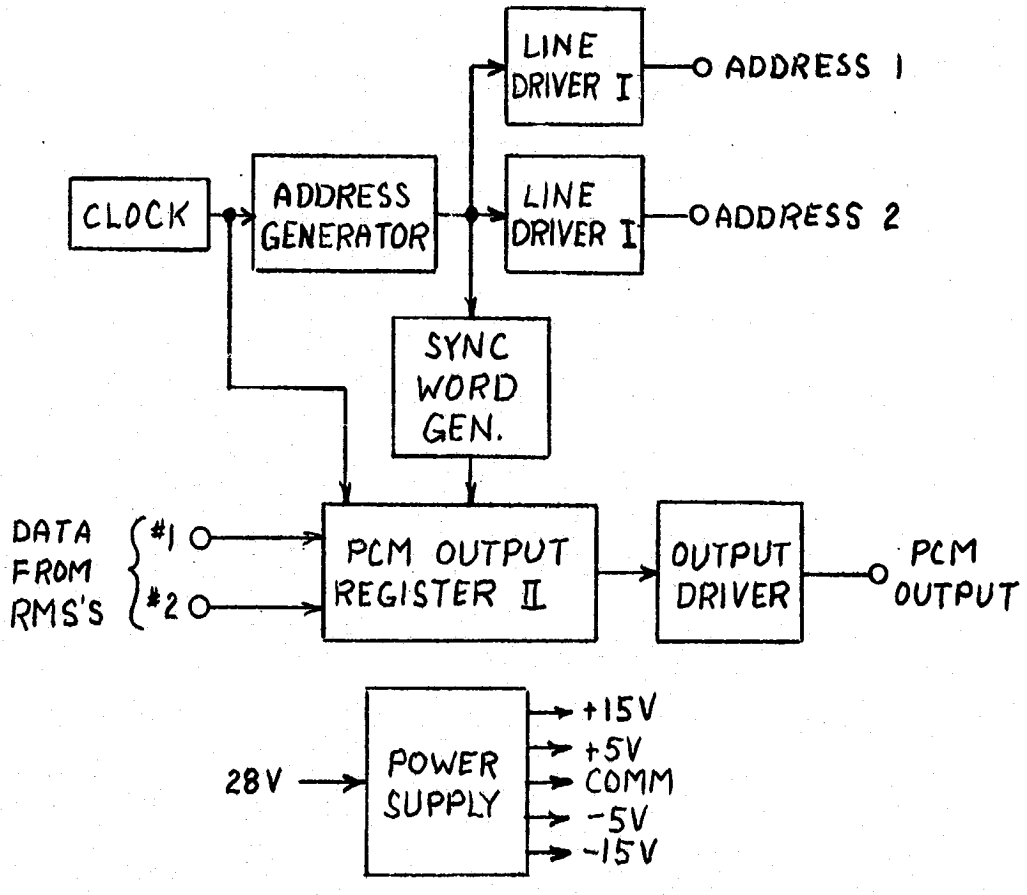


Figure B-17, Central Control Unit II

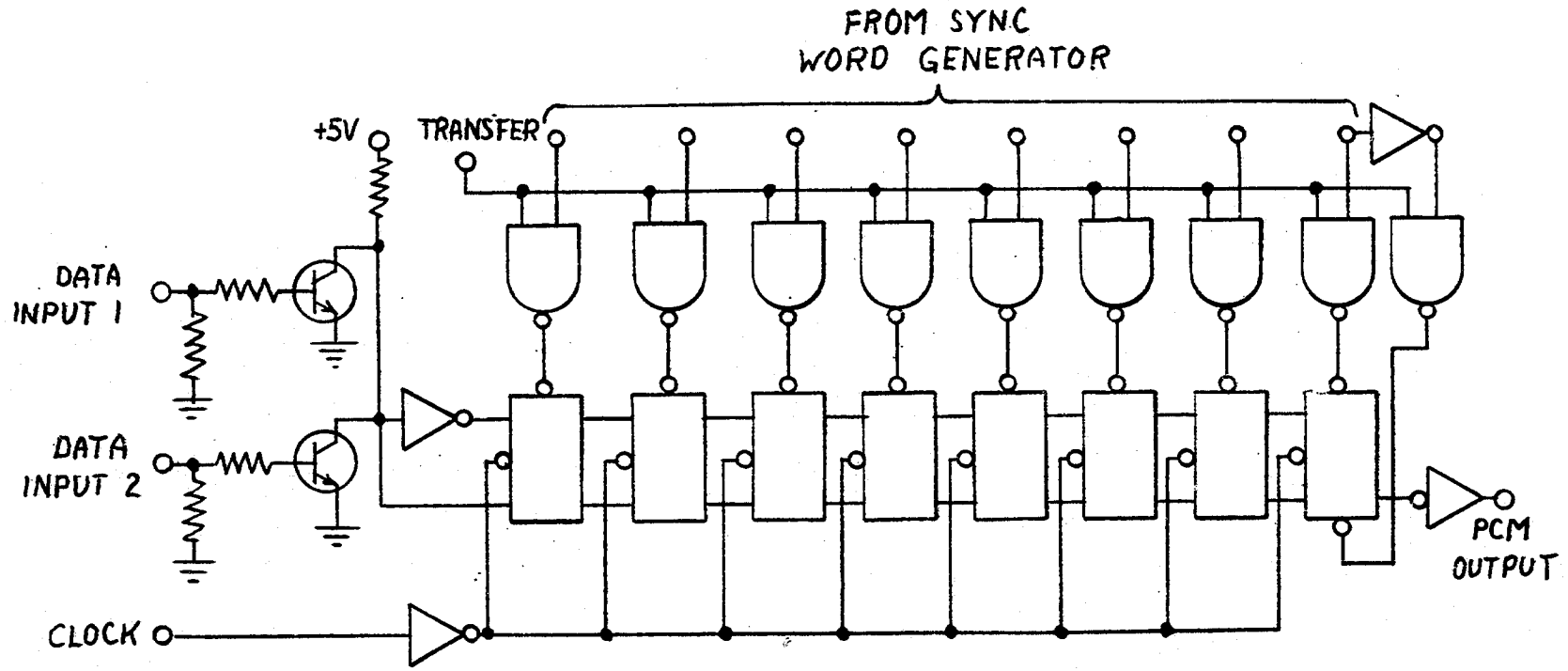


Figure B-18, PCM Output Register II & Output Driver

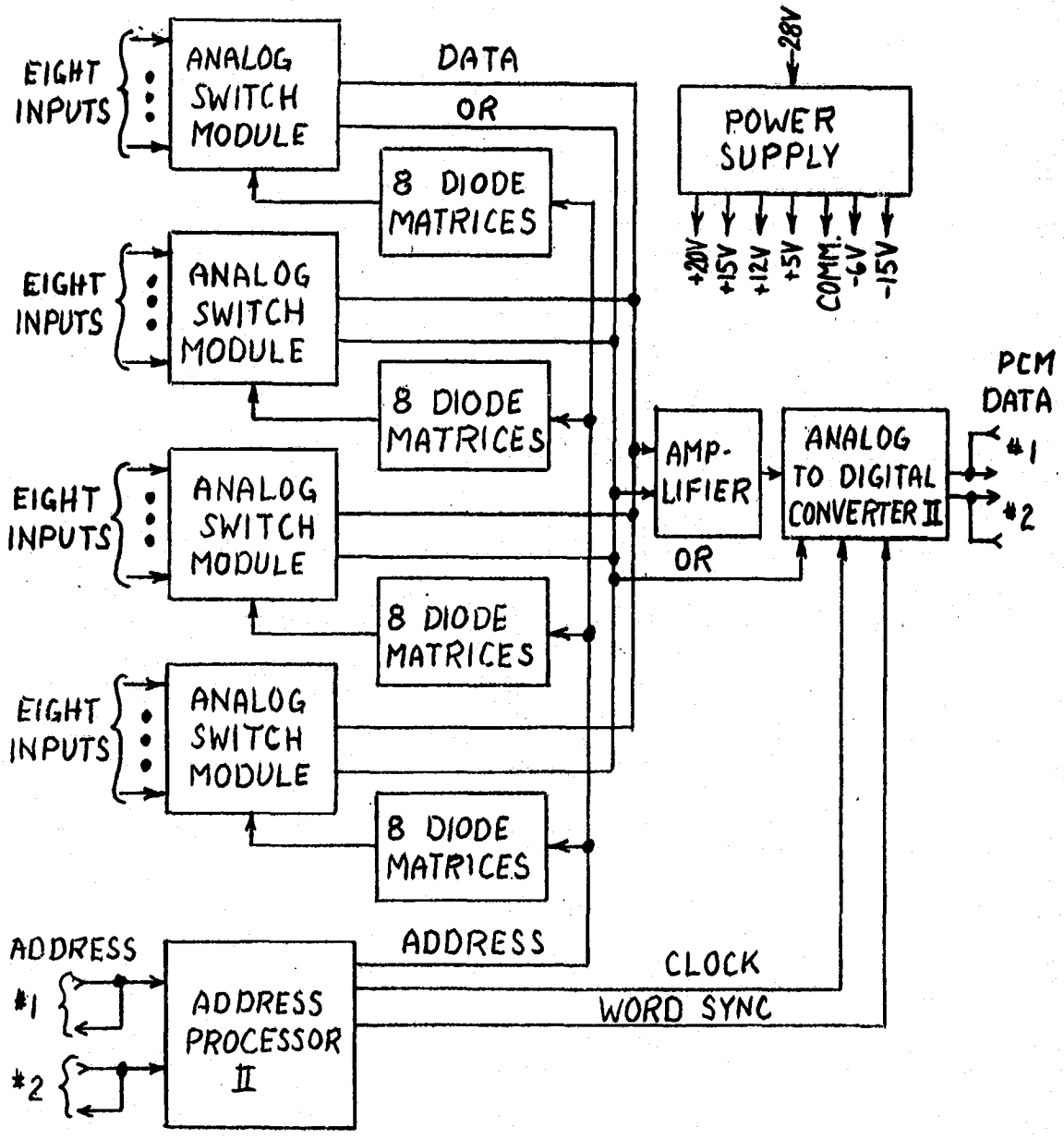


Figure B-19, RMS II

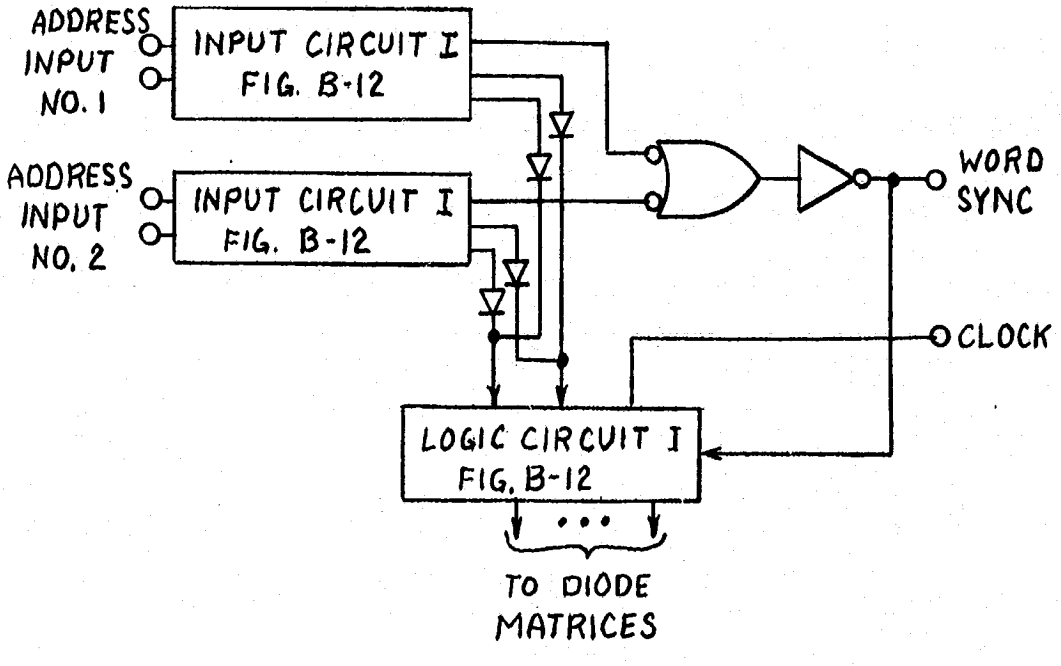


Figure B-20, Address Processor II

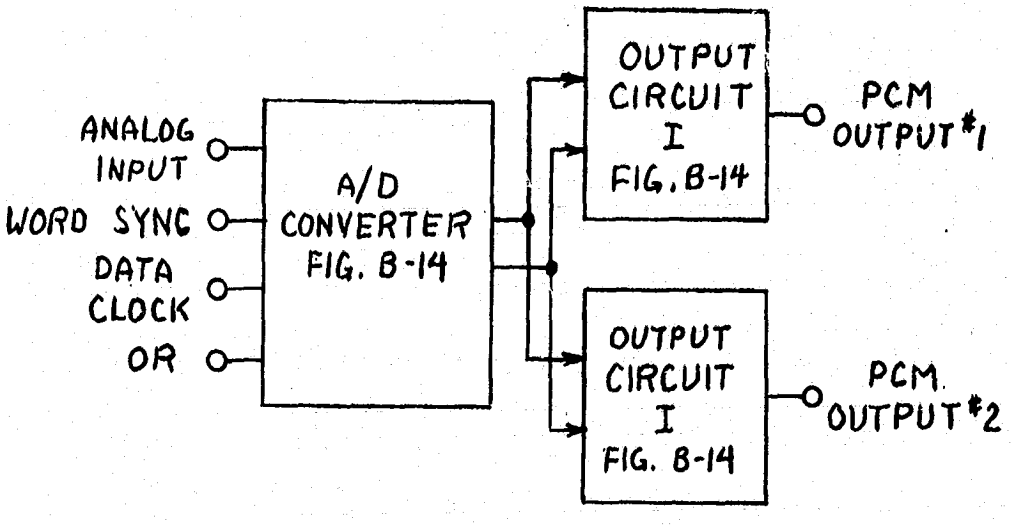


Figure B-21, A/D Converter II

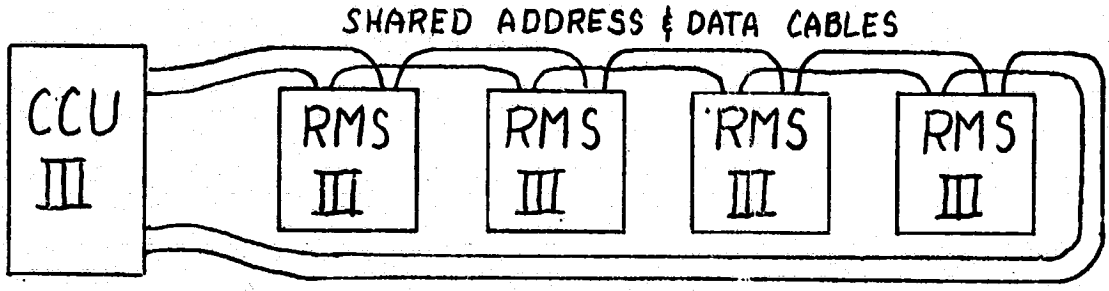


Figure B-22, Block Diagram, Configuration III

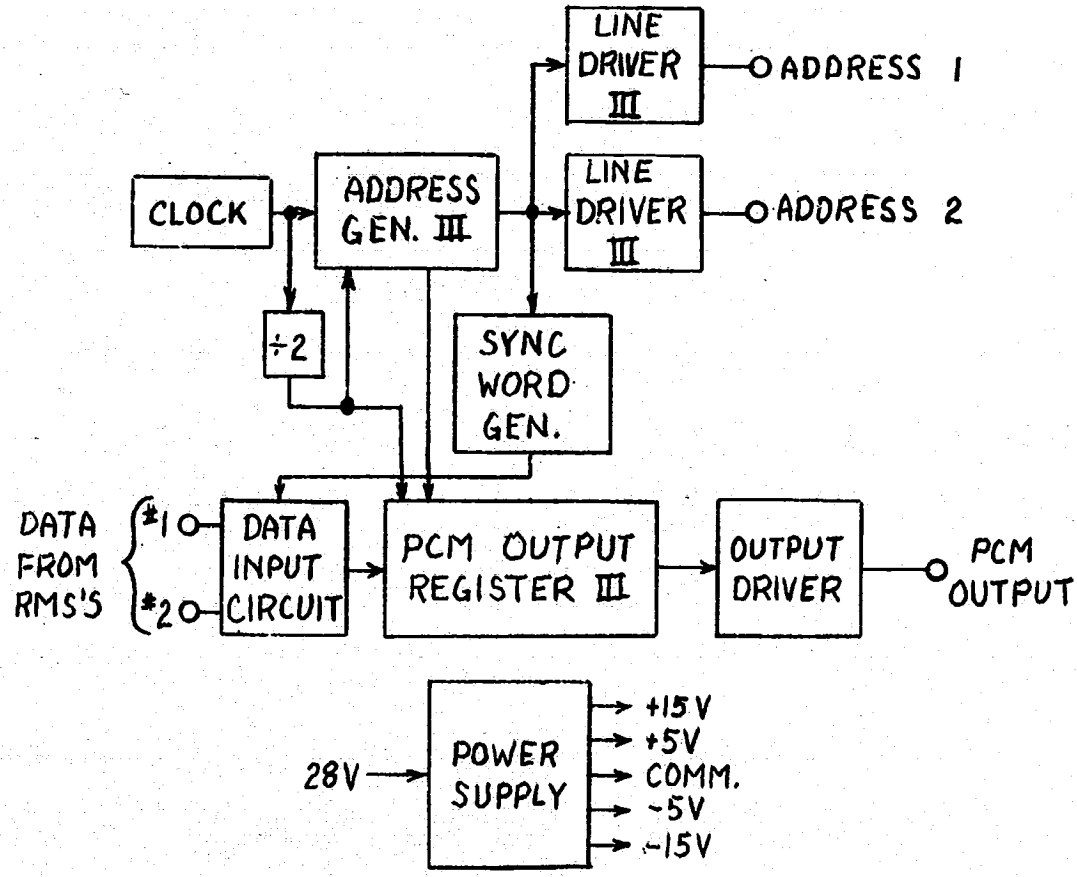


Figure B-23, Block Diagram, CCU III

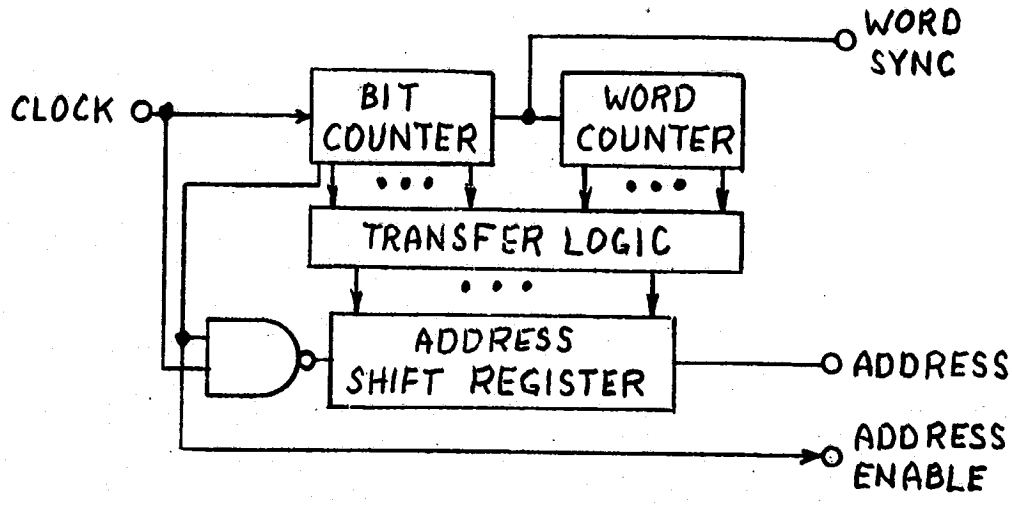


Figure B-24, Address Generator III

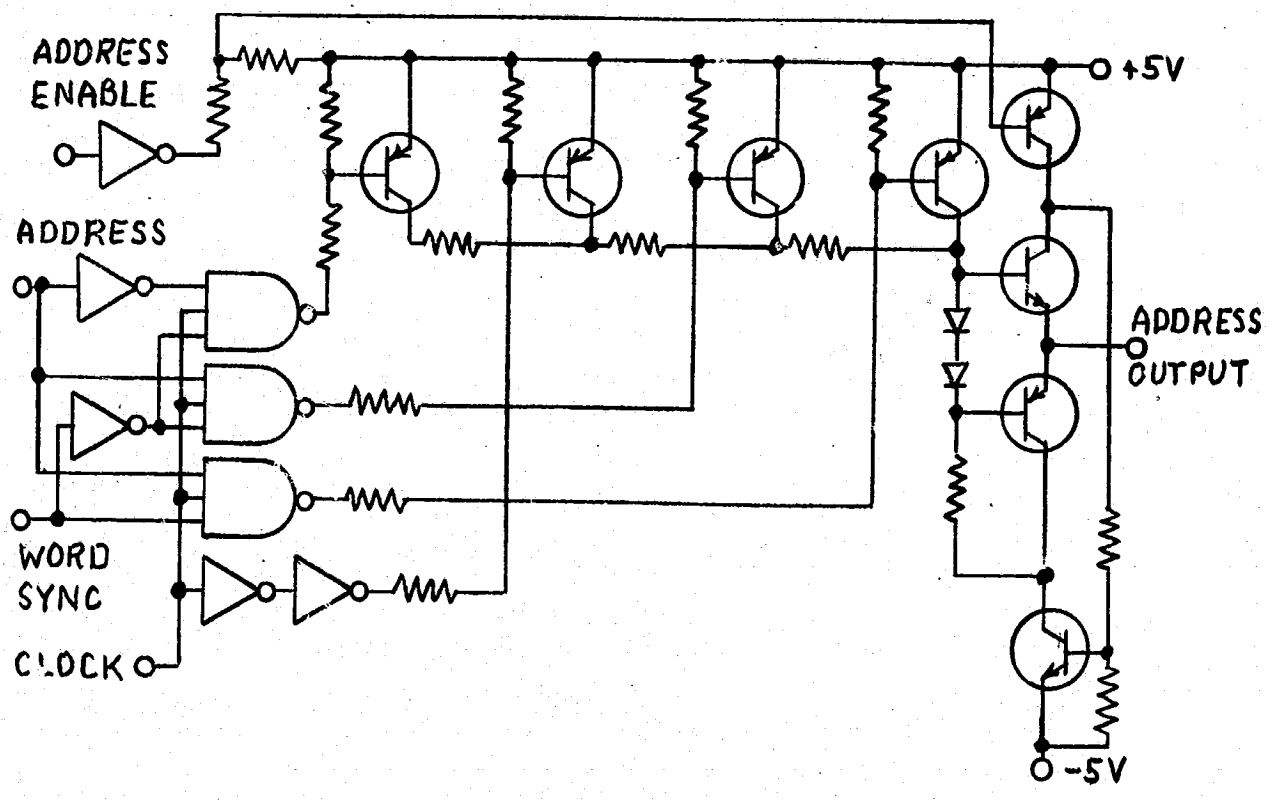


Figure B-25, Address Line Driver III

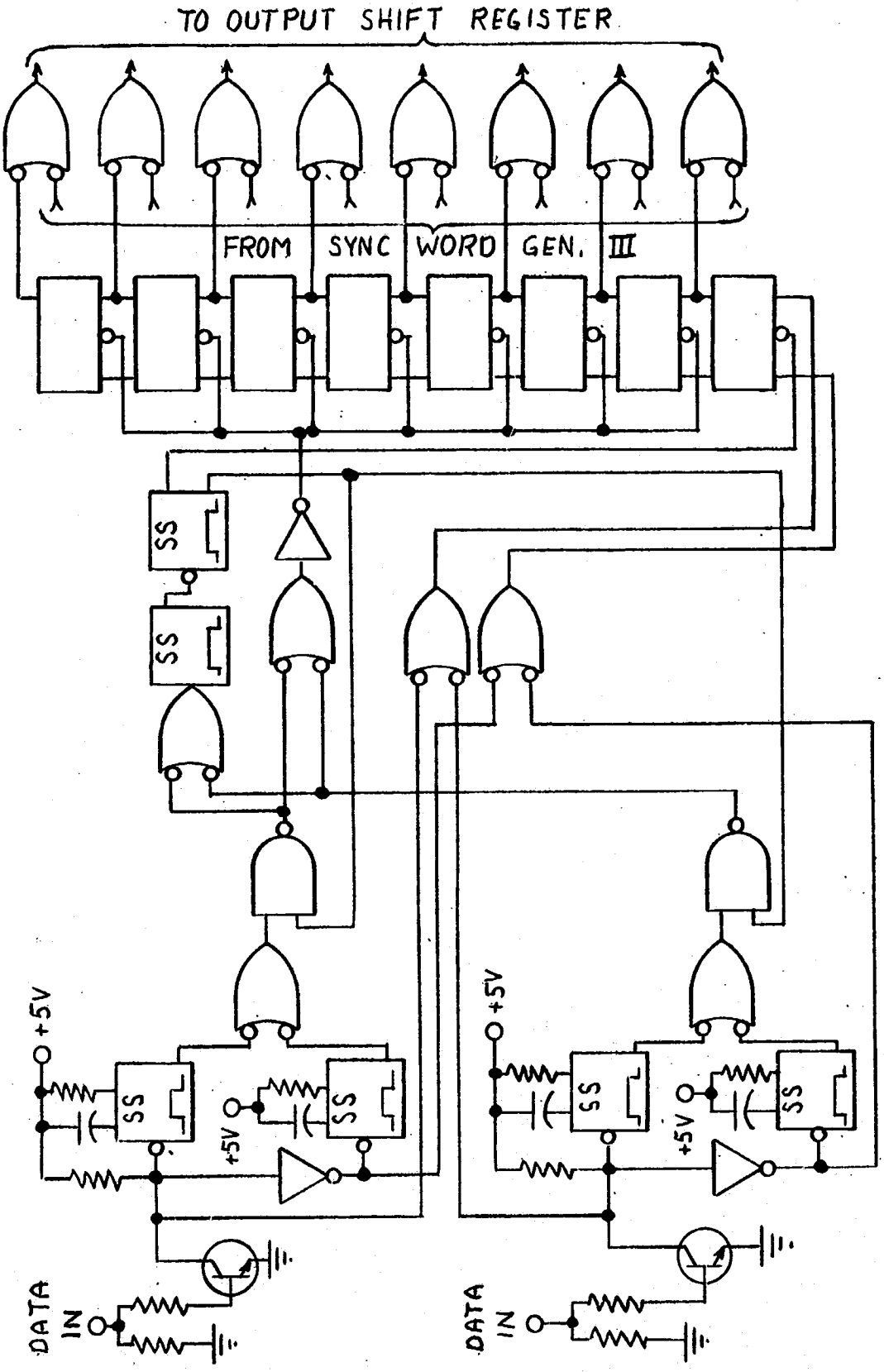


Figure B-26, Data Input Circuit III

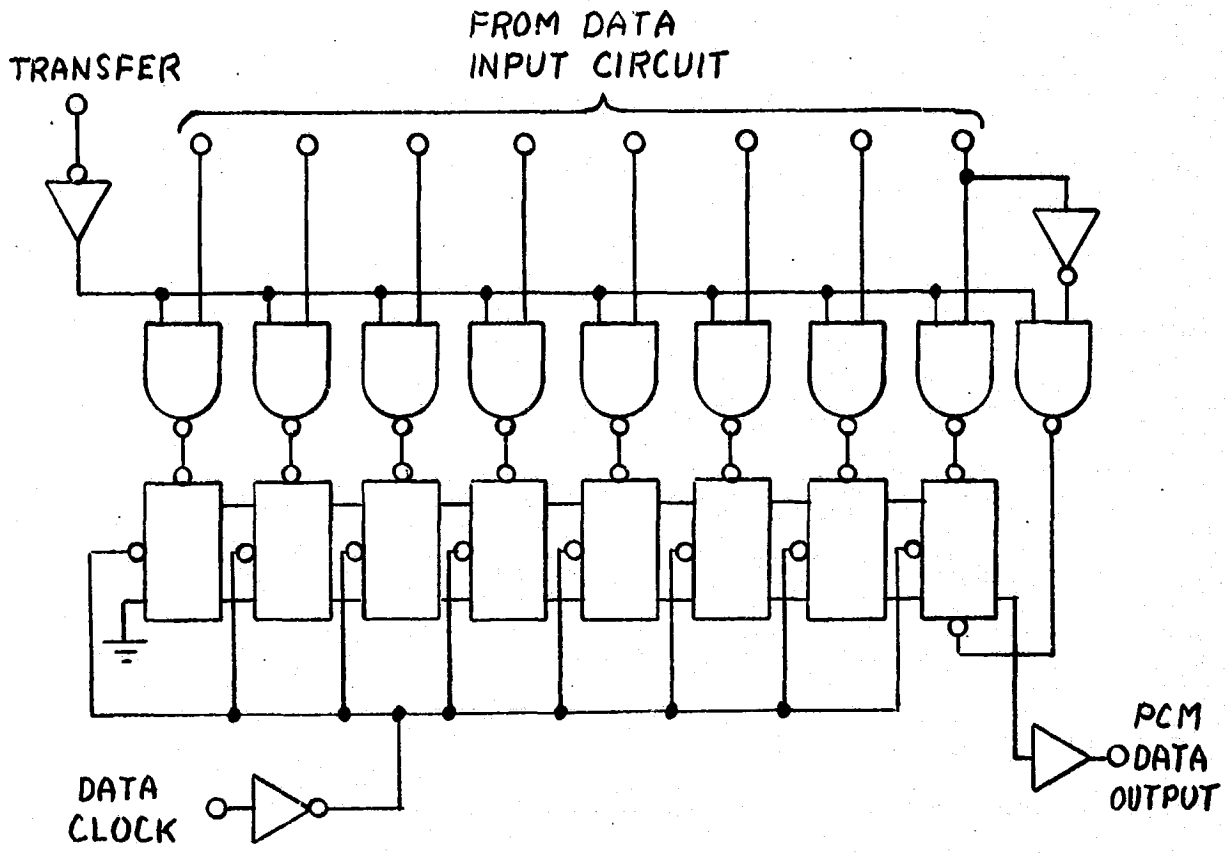


Figure B-27, PCM Output Register III & Output Driver

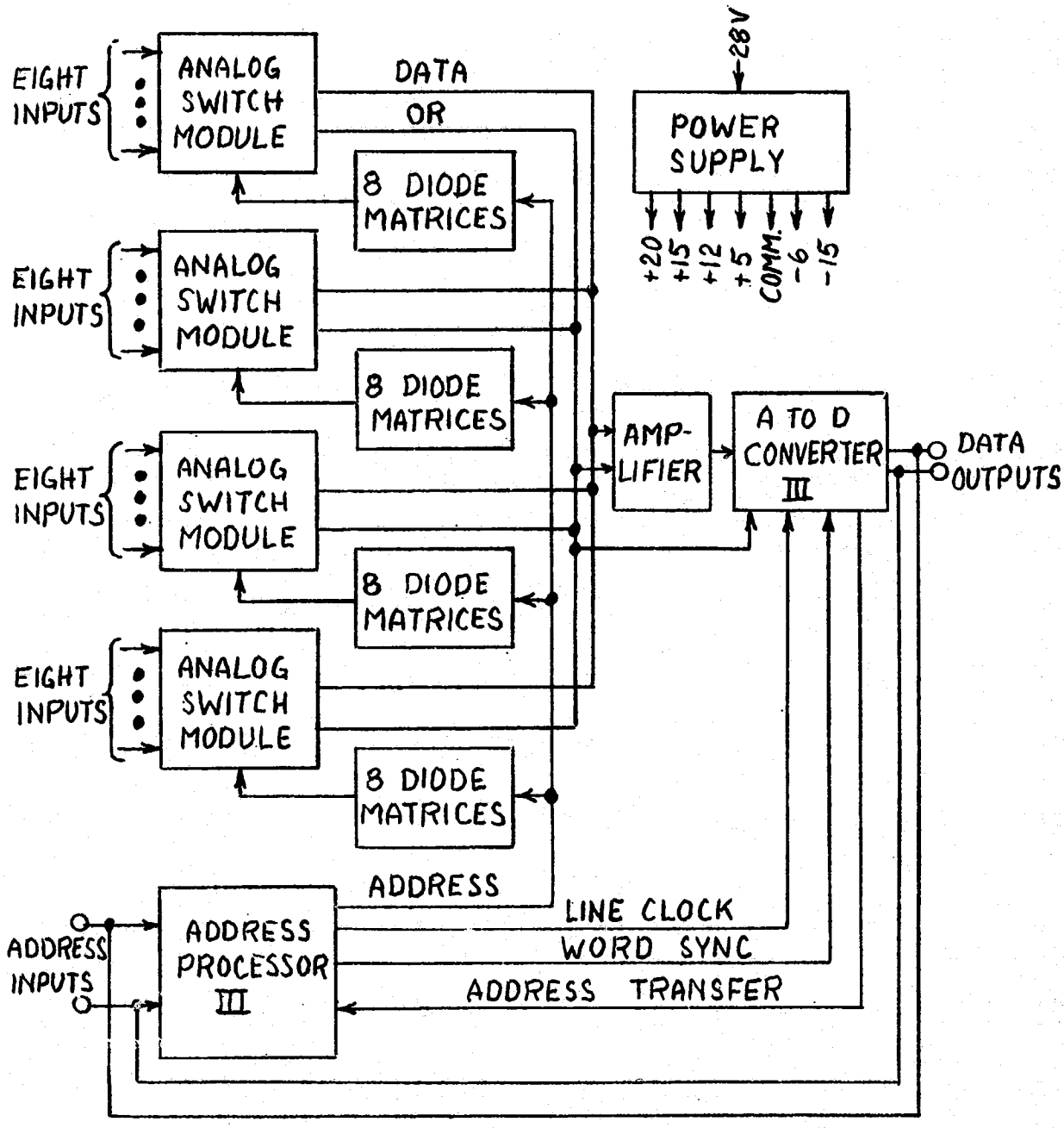


Figure B-28, RMS III

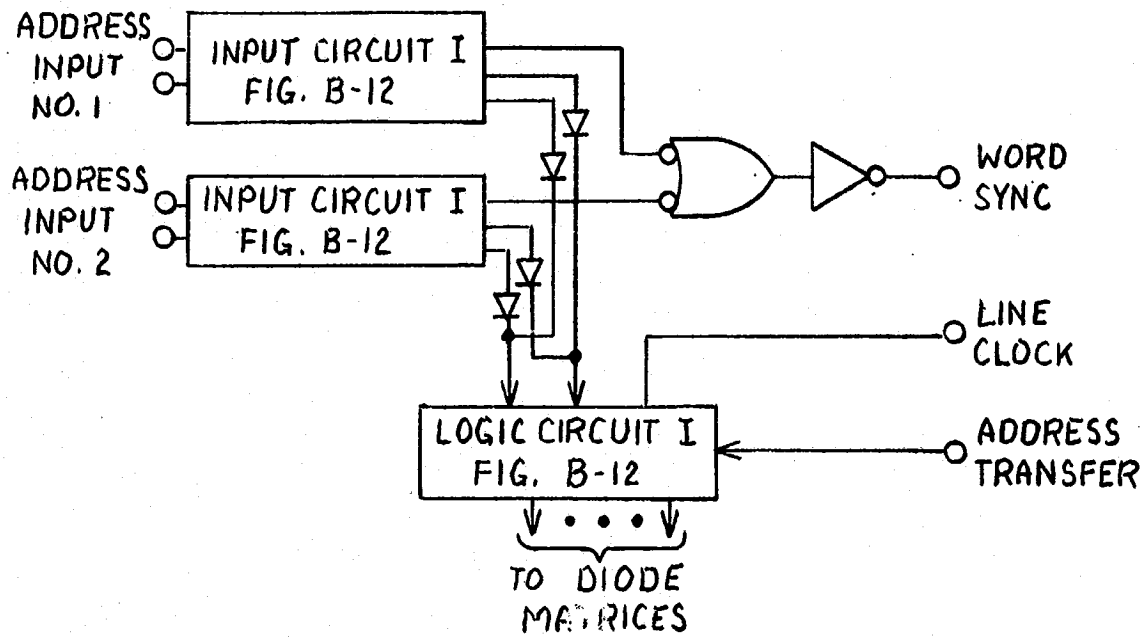


Figure B-29, Address Processor III

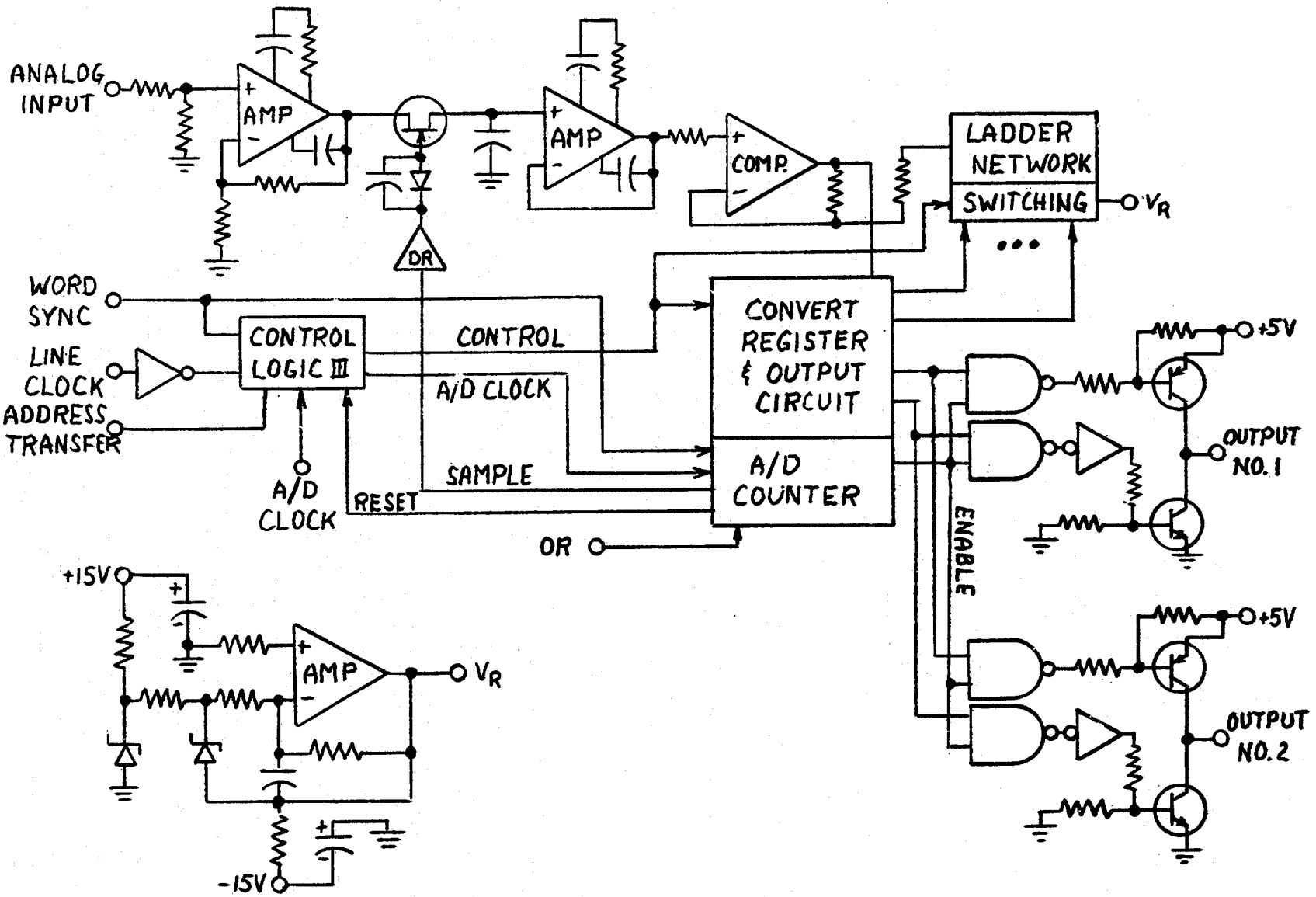


Figure B-30, A/D Converter III

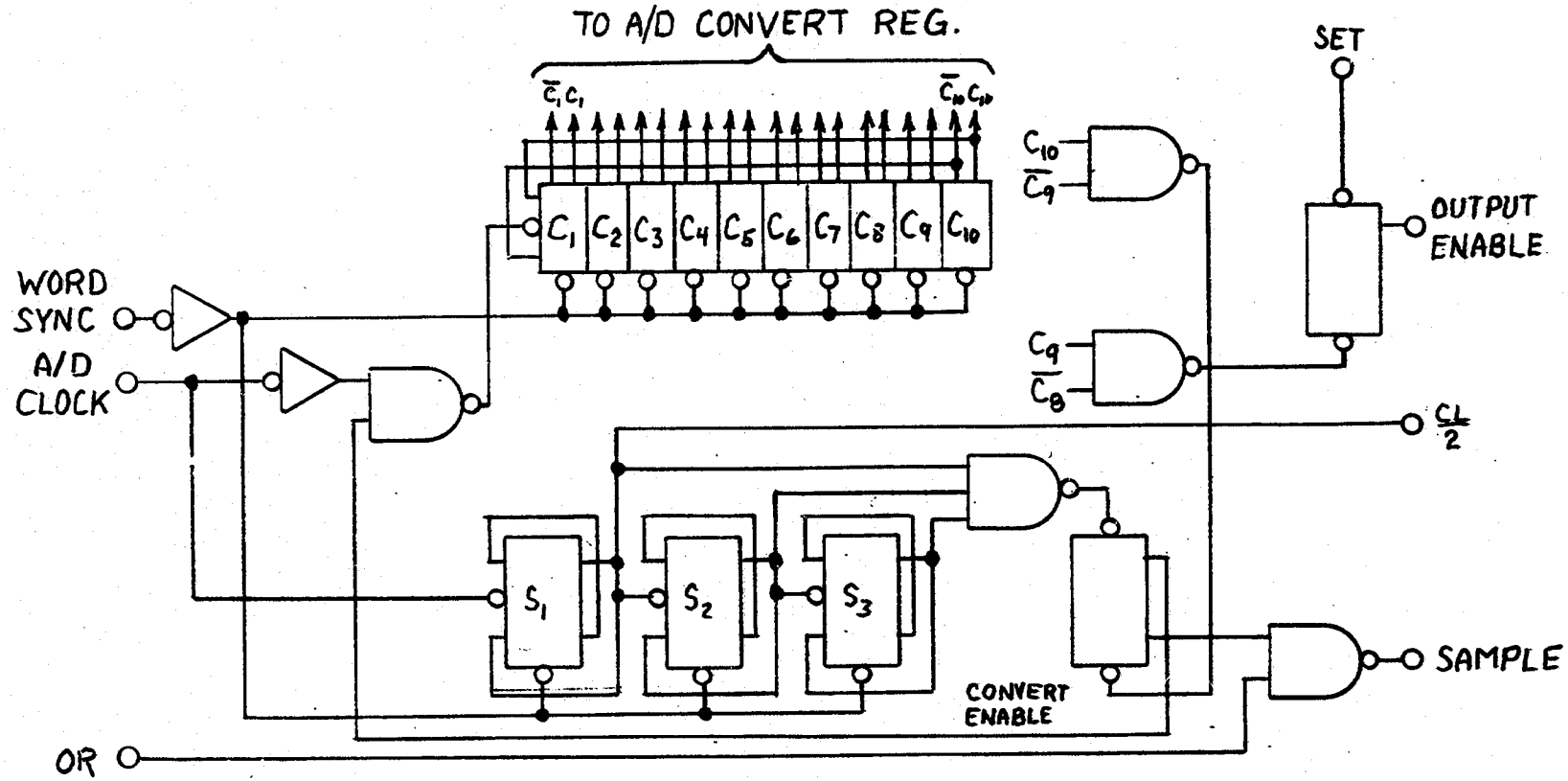


Figure B-31, A/D Converter III Counter

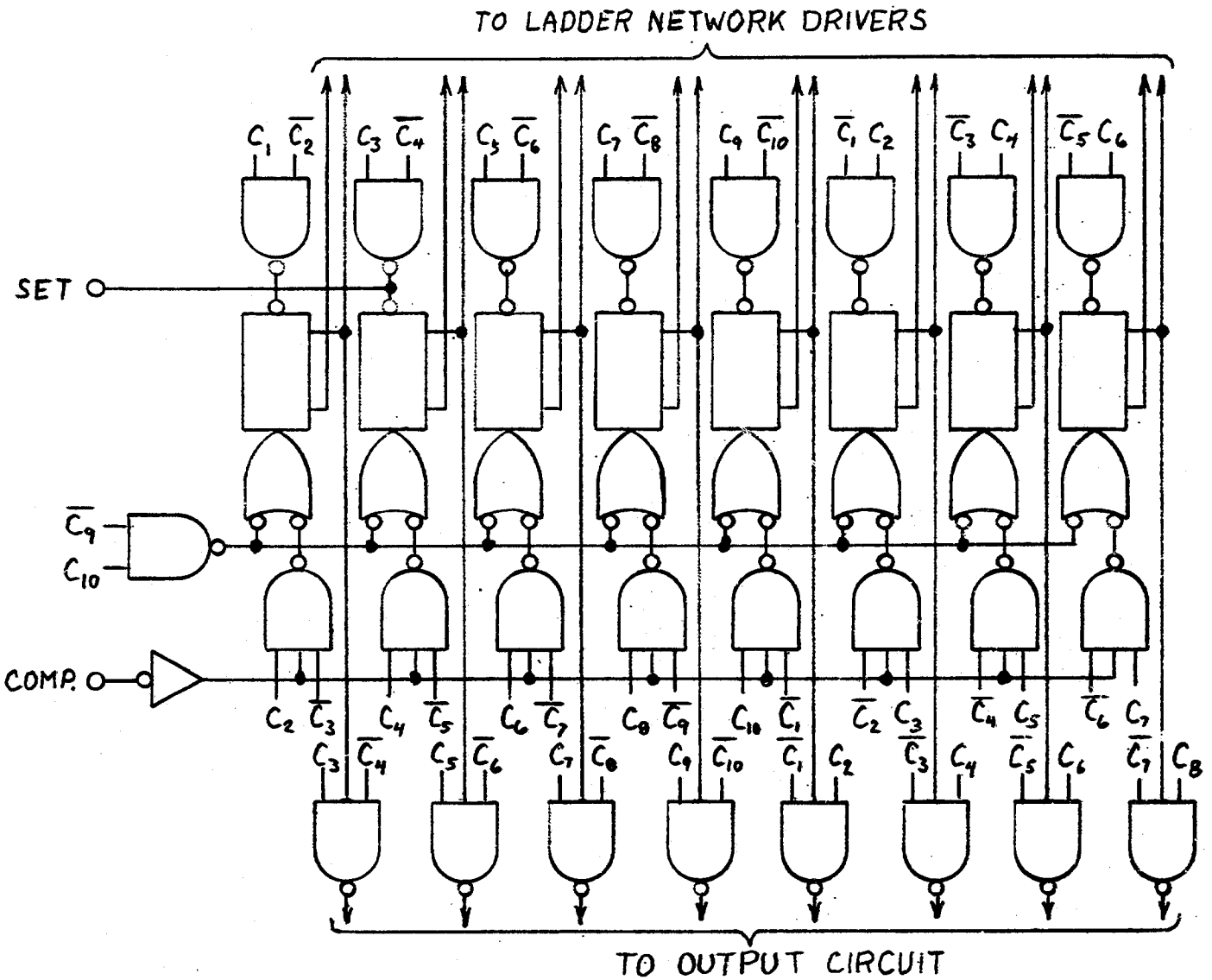


Figure B-32, A/D Converter III Convert Register

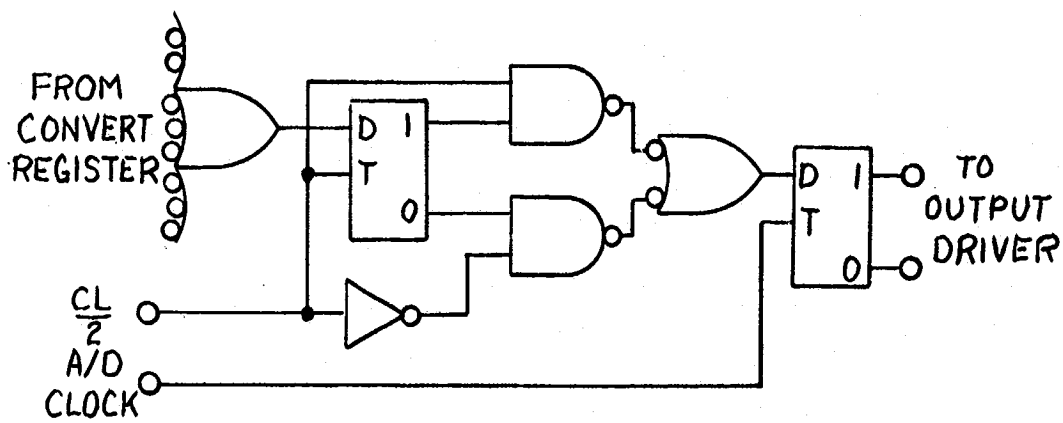


Figure B-33, A/D Converter III Output Circuit

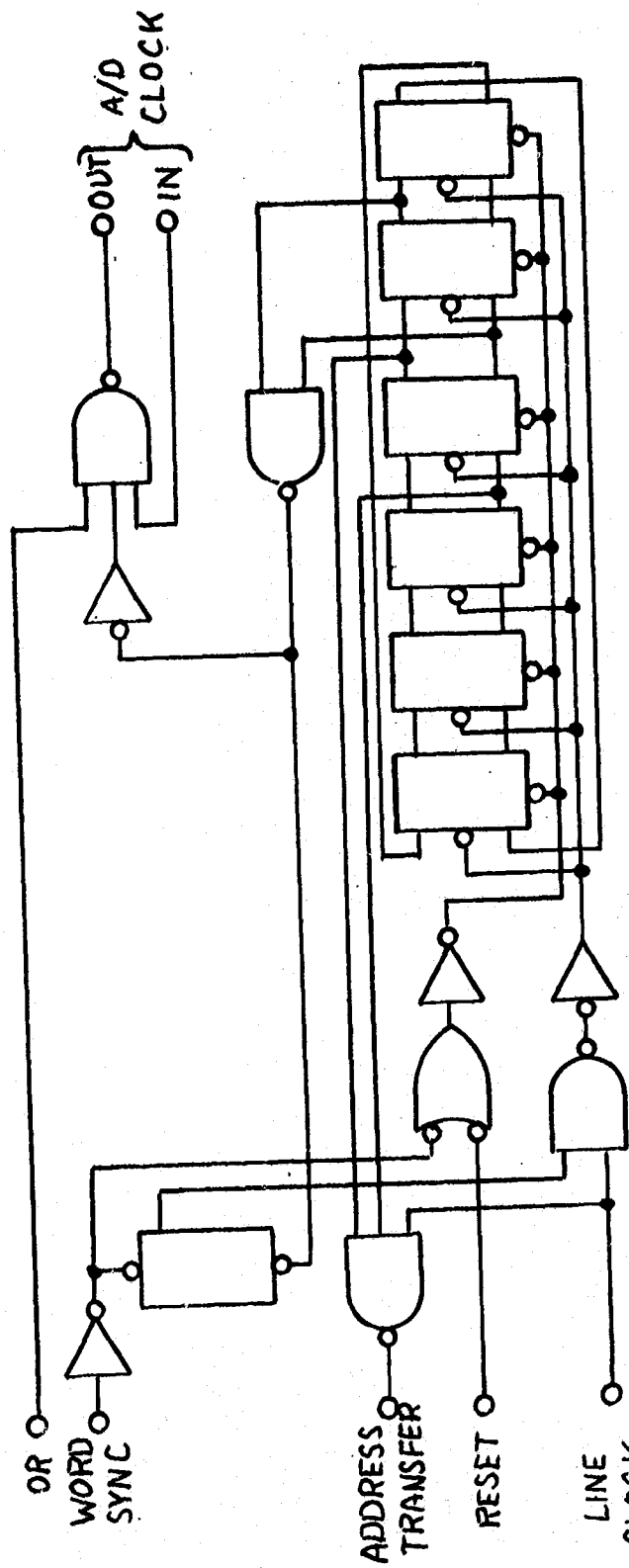


Figure B-34, A/D Converter III Control

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